We feel that the errors are due to fabrication error because the error does not repeat itself in the other three chips.

Speed Test: The chip was tested at 34MHz sampling frequency. The chip worked when tested with a clock cycle greater than 117.6 ns and failed when tested with a clock cycle of 58.8 ns. Since Omnilab is not capable of measuring clock cyles in between 117.6 ns and 58.8 ns, we were unable to test the chip in that interval to get a more precise result.

Submitted by Daniel Go (dango@rice.edu) and Jing Zhao (jingzhao@rice.edu)

Further information on this project may be obtained on the WWW at http://www.owl-net.rice.edu:80/~jingzhao

Fab -ID N5CRBG1

P-P:

Description:

8 bit calculator that can compute addition, subtraction, NOT, AND, OR, and XOR as well as shift left and right 4 bits and append up to 4 bits to the shifted number. Furthermore, this 8 bit calculator has an output feedback loop so the output can be remembered and operated on in subsequent clock cycles.

The 8 bit numbers for addition and subtraction operations are in 2's complement form.

The chip is built from several subcells. The main operation blocks are the arithmetic logic unit which computes the logic functions as well as the addition and subtraction, a block for shifting the input to the right and a block for shifting the signal to the left. The arithmetic logic unit can be further broken down into two 4 bit ALU with a carry-in and a carry-out pin.

The inputs are latched, and the operation codes are fed into a decoder which in turn activates the appropriate operation. The flow of the data in the chip is controlled by a small PLA which dictates when to reset the latches, load the data, and feedback the output.

The output from each operation is multiplexed to ensure that the output from the desired function is allowed to pass through and then latched, giving the user the option of feeding the output as one of the inputs in the next clock cycle.

Results:

Out of the 4 chips that we received 2 were completely functional, one was partially functional, and the last one was non-functional.

Reasons for Chip Failure:

For the chip that was non-functional, it was because the OUT2 pin on the output was stuck at "1". The error we felt was located in the output latch because the output was consistently high across all the operations. We feel that since this error was not present in the other three chips, that this is probably the result of a fabrication error, either a wafer error a mask error.

For the chip that was partially functional, The outputs that were incorrect were all exhibited in the Rightshift and Leftshift operations.

Rightshift fails when you want to shift more than 2 bits and you want to add a 1 as the leftmost bit corresponding to IN9, because IN9 is stuck at zero for the rightshift bank of shifters.

Leftshift fails when you want to shift more than 1 bit and you want to add a 1 as the rightmost bit corresponding to IN8 and IN10, because both IN8 and IN10 are stuck at zero for the leftshift bank of shifters.

5.0 Speed Results of the Chip

During Elec 422, we calculated using spice that our chip has a maximum rise time of 70ns.

The results for the actual chip what we measured was shown below:

Speed Test Results

Predicted Speed : 70 ns.

TABLE 3. Speed Test Results

Clock Cycle	Measured Speeds	Results
34 MHz (non-overlapping)	117.6 ns	Correct
17 MHz (overlapping)	117.6 ns	Correct
34 MHz (overlapping)	58.8 ns	In-Correct

The results agrees with what we predicted. At 58.8 ns we also may encounter the maximum frequency of the pad frame.

6.0 Additional Copy of the Mosis Report

Report Date	April 23, 1996
From	Professor Cavallaro, cavallar@rice.edu
Designer	Daniel Go and Jing Zhao
Design Description	Simple 8 bit calculator
ID	47553
P-Name	calcc

3.0 Number of chips that were functional

2 out of 4 chips were completely functional.

Chip 1 and Chip 2 are partially functional.

Chip 3 and 4 are completely functional.

3.1 Which outputs are incorrect for Chip 1

The outputs that are incorrect with Chip 1 are all exhibited in the Rightshift and Leftshift operations.

Rightshift fails when you want to shift more than 2 bits and you want to add a 1 as the leftmost bit corresponding to IN9, because IN9 is stuck at zero for the rightshift bank of shifters.

Leftshift fails when you want to shift more than 1 bit and you want to add a 1 as the rightmost bit corresponding to IN8 and IN10, because both IN8 and IN10 are stuck at zero for the leftshift bank of shifters.

We feel that the errors are due to fabrication error because the error does not repeat itself in the other three chips.

3.2 Which outputs are incorrect for Chip 2

In Chip 2, the output bit, OUT2, is stuck at one for all the operations. We feel that since OUT2 is stuck at one for all the operations, the error must be in the output latch of OUT2.

We feel that the errors are due to fabrication error because this error does not repeat in itself in the other three chips.

4.0 Comparison of results with IRSIM results

The results of the Omnilab simulation when compared to the IRSIM results were identical as the following graphs will show:

The description of the test vectors we used are the following:

2.1 Test Vectors for the Adder/Subtractor

The test vectors are as follows:

1. loads 01001100 for A and 00101111 for B

2. Adds 01001100 to 00101111 should get 01111011 hold output.

3. Subtracts 01000011 from 01111011 should get 00111000 hold output

4. Adds 01101010 to 00111000 should get 10100010 and error, hold output

5. Subtracts 01111011 from 10100010 should get 00100111 and error, hold output

6. Subtracts 10111001 from 00100111 should get 01101110 and error.

7. Subtracts 10111001 from 01010110 should get 1001101 and error.

2.2 Test Vectors for the Logic Circuits

The test vectors are as follows:

1. loads 10101010 for A and 00111010 for B

2. Computes 10101010 AND 00111010 should get 00101010 hold output.

3. Computes NOT 00101010 should get 11010101 hold output.

4. Computes 11010101 OR 11001100 should get 11011101 hold output

5. Computes 11011101 XOR 01010110 should get 10001011 hold output.

2.3 Test Vectors for the Shifter Circuits

The test vectors are as follows:

1. Load 00000000 into A.

2. Shift 00000000 right 4 bits add 1111 should get 11110000 and hold.

3. Shift 11110000 left 2 bits add 11 should get 11000011 and hold.

4. Shift 11000011 left 4 bits add 1100 should get 00111100 and hold.

5. Shift 00111100 right 3 bits add 001 should get 00100111 and hold.

6. Shift 00100111 right 1 bit add 1 should get 10010011 and hold.

TABLE 2. Omnilab stimulus connections

Channel	Bit	output
1	7	op2
2	0	a0
2	1	a1
2	2	a2
2	3	a3
2	4	a4
2	5	a5
2	6	a6
2	7	a7
3	0	b0
3	1	b1
3	2	b2
3	3	b3
3	4	b4
3	5	b5
3	6	b6
3	7	b7

In terms of any customization that was needed, we had to connect the output of the trigger stimulus to the reset pin of our chip. We had to do this because our the analyzer was running out of input pins.

2.0 Number and types of test vectors that are used

We used three different sets of test vectors; each set to test a different operation of the chip, the adder/subtractor, the logic circuits, and the shifters. Due to the fact that we have feedback built into this chip it is impossible to test all the possibilities and combinations.

Note that in the case of Chip 1 whose shifters failed, we developed a basic IRSIM test to diagnose the problem which consisted of no feedback and four different cases.

1. A = 11111111 shifted left 1,2,3, and 4 bits appending a zero bit each time.

2. A = 11111111 shifted right 1,2,3, and 4 bits appending a zero bit each time.

3. A = 00000000 shifted left 1,2,3, and 4 bits appending a one bit each time.

4. A = 00000000 shifted right 1,2,3, and 4 bits appending a one bit each time.

TABLE 1. Omnilab analyzer connections

Analyzer pin	Chip Pin
e3	a4
e2	a5
e1	a6
e0	a7
f7	b0
f6	b1
f5	b2
f4	b3
f3	b4
f2	b5
f1	b6
f0	b7
c7	out0
c6	out1
c5	out2
c4	out3
c3	out4
c2	out5
c1	out6
c0	out7
b7	error

TABLE 2. Omnilab stimulus connections

Channel	Bit	output
1	0	clkA
1	1	clkB
1	2	trigger/reset
1	3	load
1	4	hold
1	5	op0
1	6	op1

Simple Calculator

Elec 423

Group C : Dan Go and Jing Zhao

1.0 Description of the Omnilab Equipment:

The Omnilab equipment was set up in the standard way, as described in the "How not to get Muddled when Confronted with the Omnilab Tester for the First Time" handout. The pin connections were the following:

TABLE 1. Omnilab analyzer connections

Analyzer pin	Chip Pin
d7	clkA
d6	clkB
d5	trigger/reset
d4	load
d3	hold
d2	op0
d1	op1
d0	op2
e7	a0
e6	a1
e5	a2
e4	a3