

# ELEC 326: Homework 4

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Due in DH 3029 by 5pm on Friday, October 30<sup>th</sup>, 2009

1. Exercise 2.26 from the textbook. Only Boolean equations are necessary!
2. Exercise 2.30 from the textbook.
3. (From a past exam) **Ones counters:** Build a circuit that counts the number of ones in a 8-bit wide bus using half-adders and full-adders. For example, if the input is 11001100, your design must output 0100 since there are four ones in the input. Treat the adders as black-boxes with  $a$ ,  $b$ , and  $carry\_in$  inputs and  $sum$  and  $carry\_out$  outputs. (Of course, the half-adders will not have a  $carry\_in$  input.) Minimize the number of adders that you need in your design.
4. **Sorting networks:** When sorting lists of some specific size, sorting networks are often employed. Sorting networks only use compare-exchange, i.e., comparator operations. A compare-exchange operation on the pair  $\{x, y\}$  does the following:

```
if (x > y) { t = x; x = y; y = t; }
```

The following are some properties of sorting networks, described with respect to the graphical representation of sorting networks in Fig. 1, which is a sorting network for 8 inputs.

- A sorting network is usually made up of a series of columns, and each column contains a number of comparators connected in parallel.
- A horizontal line represents each input of the sorting network and a connection between two lines represents each comparator which compares the two elements and exchanges them if the one on the upper line is larger than the one on the lower line. The input of the sorting network is on the left of the representation.
- Each column of comparators perform a permutation, and the output obtained from the final column is sorted in increasing or decreasing order. In the figure, elements at the output are sorted such that the largest element migrates to the bottom line.
- The depth of a sorting network is the number of columns it contains. In other words, the depth is defined as the number of parallel steps that it takes to sort any input, given that in one step, disjoint compare-exchange (i.e., comparator) operations can take place simultaneously.
- The length of a sorting network is the number of comparators that are used.
  - (a) Design an optimal comparator unit that is used in a sorting network using CMOS gates.

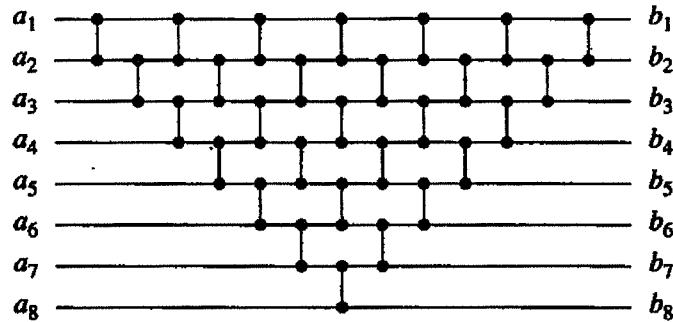


Figure 1: 8-input sorting network

- (b) Design (as optimal as possible) sorting networks with 3 and 4 inputs. The best known results {depth, length (number of comparators)} for 3 and 4 inputs are {3, 3} and {3, 5} respectively. Show that your solution works.
5. Implement the Boolean function  $\sum_{a,b,c,d} (0, 3, 4, 7, 14, 15)$  using the 74LS139 decoder and as few additional gates as possible.
6. We say a variable  $x$  is in the **support** of a Boolean function  $f$  if  $f_x \neq f_{\bar{x}}$ . How many Boolean functions of three variables have three variables in their support?  
 Note that a Boolean formula involving three variables does not necessarily imply that all three variables are in the support of the function denoted by that formula; for example, consider  $f = xyz + xy\bar{z}$  that can be simplified to  $f = xy$ .
7. (From a past exam) Design a 4-to-10 decoder that receives binary-encoded inputs  $i_3i_2i_1i_0$  over the range 1–10 (0001–1010). Your solution must provision for an active low EN (enable) input in addition to  $i_3i_2i_1i_0$ , and the data outputs  $d_{10}d_9 \cdots d_1$  must also follow the active low convention. For example, if the input is 0101, the output  $d_{10}d_9 \cdots d_1$  for EN equals 0 (EN equals 1) must be 1111101111 (1111111111).  
 Your solution must use a minimum number of 74LS138 and 74LS139 decoders, the combined data-sheet for which follow. All connections for input/output must be clearly marked on a schematic for full credit.  
**Note:** Two pages from the data-sheets for the 74LS138 and 74LS139 decoders follow at the end of this homework.
8. Anonymous course feedback. Please provide open format feedback, i.e., “say what you want to” feedback about ELEC 326 on a separate page for easy access. I expect to receive as many forms as there are students enrolled, so there is no getting around this exercise.

**Practice problems (not graded)**

9. Prove the following properties of cofactors:
- (a)  $((f)_x)_y = ((f)_y)_x$
  - (b)  $(f + g)_x = f_x + g_x$

$$(c) (fg)_x = f_x g_x$$

$$(d) (\overline{f})_x = \overline{(f_x)}$$

10. (From a past exam) A Boolean function is symmetric in its inputs if all that matters is the number of bits that have to be set to logic 1 for it to be TRUE. In other words, the order of the inputs to the Boolean function is irrelevant. For example, the Boolean functions  $(a + b)$  as well as  $(\bar{a} + \bar{b})$  of 2 inputs are both symmetric.  $(a + b)$  is symmetric because you just need to know that at least 1 bit must be set to logic 1 for it to be TRUE. Similarly,  $(\bar{a} + \bar{b})$  is symmetric because you just need to know that no more than 1 bit must be set to logic 1 for it to be TRUE.

**Hint:** Start by looking at other examples of symmetric functions on two inputs. Ask yourself if  $ab$  is symmetric. And think carefully about our friends, the constant 0 and 1 functions.

- (a) List all symmetric Boolean functions of 3 inputs
- (b) How many symmetric Boolean functions can you construct given  $n$  inputs? I need to see a constructive argument, not just a number or closed-form expression.

## DM74LS138 • DM74LS139 Decoder/Demultiplexer

### General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

### Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - DM74LS138 21 ns
  - DM74LS139 21 ns
- Typical power dissipation
  - DM74LS138 32 mW
  - DM74LS139 34 mW

### Ordering Code:

Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
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Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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