

# Technology exploration for graphene nanoribbon FETs

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## Abstract

Graphene nanoribbon FETs (GNRFETs) are promising devices for beyond-CMOS nanoelectronics because of their excellent carrier transport properties and potential for large scale processing and fabrication. This paper combines atomistic quantum transport modeling with circuit simulation to perform technology exploration for GNRFET circuits. A quantitative study of the effects of variations and defects on the performance and reliability of GNRFET circuits is also presented. Simulation results indicate that whereas GNRFET circuits promise higher performance, lower energy consumption, and comparable reliability at similar operating points to scaled CMOS circuits, they are more susceptible to variations and defects. The results also motivate significant engineering, modeling, and simulation challenges facing the device and CAD communities involved in graphene electronics research.

**Categories and Subject Descriptors:** B.7.1 [Integrated circuits]: Types and Design Styles—Advanced technologies

**General Terms:** Design, Performance, Reliability

**Keywords:** Graphene nanoribbons, variability, defects

## 1. Introduction

Graphene, which is a monolayer of carbon atoms packed into a two-dimensional honeycomb lattice, has emerged as a promising candidate material for beyond-CMOS nanoelectronics. Graphene-based devices offer high mobility for ballistic transport, high carrier velocity for fast switching, monolayer thin body for optimum electrostatic scaling, and excellent thermal conductivity [1–6]. The potential to produce wafer-scale graphene films with full planar processing for devices promises high integration potential with conventional CMOS fabrication processes, which is a significant advantage over carbon nanotubes (CNTs) [6]. Although two-dimensional graphene is a zero band-gap semi-metal, a band-gap opens when a field-effect transistor (FET) channel is fabricated on a nanometer-wide graphene nanoribbon (GNR) [6–9]. Unlike CNTs, which are mixtures of metallic and semiconducting materials, a recent experiment [9] demonstrated that all sub-10nm GNRs are semiconducting due to the edge effect, which make them more attractive for electronic device applications.

This paper presents extensive results on technology exploration for GNRFET circuits. It couples atomistic quantum transport modeling in intrinsic GNRFETs with a circuit simulator that includes parasitics and non-idealities that are necessary to capture extrinsic

effects in fabricated GNRFETs. At the device level, GNRFETs are simulated by self-consistently solving an atomistic quantum transport equation based on the non-equilibrium Green's function (NEGF) formalism with the 3D Poisson's equation. These rigorous simulations provide  $I$ - $V$  and  $Q$ - $V$  data for intrinsic GNRFETs, which are integrated into a circuit-level simulation framework based on lookup tables for technology exploration of GNRFET circuits. The simulator is used to study the delay, power, energy, and noise margins of representative GNRFET circuits including inverters, ring oscillators, and latches. Results indicate that GNRFETs offer significant gains over scaled CMOS at the 22, 32, and 45nm nodes, with over 40–168X improvement in the energy-delay product at comparable operating points.

Significant technical challenges, however, remain to be met. Due to the atomically thin and nanometer-wide geometries of GNRs, variability and defects are projected to have a larger impact on circuit performance and reliability in comparison to conventional silicon devices. The framework is extended to perform a quantitative study of the effects of variations and defects in intrinsic GNRFETs on the performance and reliability of GNRFET circuits. Independent variations in GNR width, which is the most common source of variation, and independent charge impurities in the gate oxide, which is the most common source of defects are considered in this paper. Variation in GNR width affects GNRFET  $I_{on}/I_{off}$  non-linearly, which in turn impacts circuit performance, power, and noise margins. Simulation results indicate variation in GNR width can increase the delay, static power, and dynamic power of inverters by 6–77%, 313–643%, and 37–215% respectively, while reducing the noise margin by 27–80%. Charge impurities affect intrinsic GNRFET characteristics non-linearly and in an asymmetric manner depending upon the polarity of the charge. Simulation results indicate that charge impurities can increase the delay, static power, and dynamic power of inverters by 8–92%, 11–37%, and 5–19% respectively, while reducing the noise margin by 14–40%. When simultaneous variations in width and charge impurities are considered, variations in width dominate though the effects are exacerbated by the presence of charge impurities.

Latch noise margins and static power also exhibit significant sensitivity to variations and defects, with near-zero noise margins and over 5X increase in static power in the worst case. Low noise margins may result in higher error rates than scaled CMOS, though the redundancy required for ECC as well as the high static power may be off-set by the advantages of high density and low power that GNRFETs offer over scaled CMOS. In summary, results show that graphene-based electronics has the potential for smaller, faster, and lower energy switches than scaled CMOS. The results also motivate significant engineering, modeling, and simulation challenges facing the device and CAD communities to make the performance and reliability of GNRFETs suitable for large scale integration.

This paper is organized as follows. Section 2 provides a background in quantum simulation of intrinsic GNRFETs. Section 3 describes technology exploration for GNRFET circuits based on a

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large-signal circuit model for extrinsic GNR-FETs. Sections 4 and 5 discuss how variations and defects impact the performance and reliability of GNR-FET circuits. Section 6 is a conclusion.

## 2. Simulation of intrinsic GNR-FETs

As devices scale with technology, the widely used compact modeling and simulation approach is unable to capture several important features of device physics including quantum effects. A powerful quantum transport simulation framework based on the non-equilibrium Green's function (NEGF) formalism provides an ideal approach for bottom-up device modeling and simulation [10] for the following reasons: (1) atomistic descriptions of devices can be readily implemented, (2) open boundaries can be rigorously treated, and (3) multi-phenomena (e.g., inelastic scattering and light emission) can be modeled.

Figure 1 summarizes the procedure to apply the NEGF approach to a generic transistor. The transistor channel, which can be a piece of silicon, a GNR, a nanowire, or a single molecule, is connected to the source and drain contacts. The gate modulates the conductance of the channel. One first identifies a suitable basis set and derives the Hamiltonian matrix  $\mathcal{H}$  for the isolated channel. Then, the self-energy matrices  $\Sigma_1$ ,  $\Sigma_2$ , and  $\Sigma_S$  are computed. The self-energy matrices describe how the channel couples to the source contact, the drain contact, and the dissipative processes. Next, the retarded Green's function, including self-consistent electrostatic potential  $\mathcal{U}$ , is computed as

$$G^r(E) = [(E + i0^+)I - \mathcal{H} - \mathcal{U} - \Sigma_1 - \Sigma_2 - \Sigma_S]^{-1}. \quad (1)$$

Finally, the physical quantities of interest, such as the charge density and current, are computed from the Green's function.

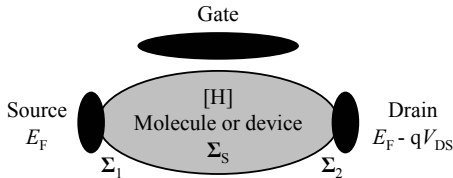


Figure 1: NEGF formalism for a generic transistor

The NEGF formalism has been applied to simulate quantum transport in various nanoelectronic devices recently. A rigorous atomistic simulation based on the NEGF formalism is computationally expensive due to its atomistic observation. However, efficient computational algorithms have been implemented to make routine device simulation and design possible on a personal computer.

In this paper, the DC characteristics of ballistic GNR-FETs are simulated by solving the Schrödinger equation using the NEGF formalism in the atomistic  $p_z$  orbital basis set self-consistently with Poisson's equation. Because the electric field varies in all dimensions for the simulated device structure, the 3D Poisson's equation is used and numerically solved using the finite element method (FEM). FEM is efficient to treat a device with multiple gates because it can easily handle an arbitrary grid for complex geometry. A  $p_z$  orbital coupling parameter of 2.7 eV is used and energy relaxation at the edges is treated according to *ab initio* calculations [11].

The simulations in this paper consider a 15 nm-long armchair-edge GNR (A-GNR) as the channel material, and the GNR width is varied from  $N=9$  to  $N=18$ , where  $N$  denotes GNR index [12]. Double gate geometry is implemented through a 1.5 nm-thick  $\text{SiO}_2$  gate insulator ( $\epsilon_r = 3.9$ ). The source and drain contacts are metals, and the Schottky barrier height is equal to half the band-gap of the channel GNR ( $\Phi_{Bn} = \Phi_{Bp} = E_g/2$ ). The gate modulates the quantum tunneling current through the Schottky barrier at the

source end of the channel, and the device operates as a Schottky barrier FET (SBFET) [13].

The  $I$ - $V$  device characteristics for the ideal  $N=12$  GNR-FET for different drain voltages is shown in Figure 2(a). Ambipolar characteristics due to both electron and hole conduction are clearly shown, and the drain voltage exponentially increases the minimum leakage current. If  $I_{on}$  is divided by the channel width, it is  $6300 \mu\text{A}/\mu\text{m}$  for the  $N=12$  GNR-FET when  $V_D$  is 0.5 V. As drain voltage increases, SBFETs show linear behavior in the overall range of gate bias. For example, the drain current and the channel charge for  $V_D=0.75$  V are linearly proportional to  $V_G$ , whereas those for  $V_D=0.25$  V show exponential behavior in the sub-threshold region.

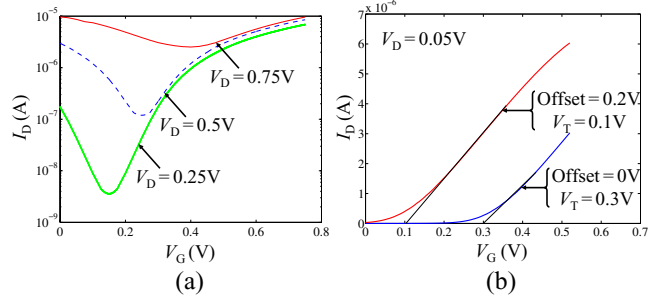


Figure 2: (a)  $I$ - $V$  characteristics and (b)  $V_T$  extraction at low  $V_D$  for ideal  $N=12$  GNR-FETs

As shown in Figure 2(a), the  $I$ - $V$  characteristics exhibit electron conduction at high gate voltages and hole conduction at low gate voltages, with minimum leakage current at  $V_G \approx V_D/2$ . The ambipolar conduction is explained by observing that the device operates as a SBFET, which is an unconventional type of transistor [13]. The threshold voltage  $V_T$  of the GNR-FET is obtained using traditional  $V_T$  extraction methods for MOS devices from the  $I$ - $V$  data [14]. When a low drain voltage  $V_{DS}$  is applied to an n-type GNR-FET, the slope of the  $I$ - $V$  curve at a high gate voltage is said to intersect the  $V_G$  axis at the threshold voltage  $V_T$ . This is illustrated for the  $I$ - $V$  curve in Figure 2(b), where the  $V_T$  is approximately 0.3V. The leakage current at  $V_G=0$  is large, but the threshold voltage of the FET can be tuned by engineering the gate metal material to shift the  $I$ - $V$  curves along the x-axis, thereby moving the point with minimum leakage current to  $V_G=0$  [15]. Note that when the off-set is applied to achieve minimum leakage,  $V_T$  changes by an amount equal to the off-set, illustrated by the  $I$ - $V$  curve for an off-set of 0.2V and a  $V_T$  of approximately 0.1V in the same figure. Finally, both n-type and p-type FETs can be achieved on the *same* GNR-FET due to the ambipolar  $I$ - $V$  characteristics. This has already been experimentally demonstrated in the context of carbon nanotube FETs [15], which exhibit ambipolar  $I$ - $V$  characteristics qualitatively similar to GNR-FETs.

## 3. Simulation of GNR-FET circuits

A simulator based on table lookup techniques was implemented to simulate circuits built with GNR-FETs. The simulator uses the drain current  $I_D(V_G, V_D)$  and channel charge  $Q(V_G, V_D)$  computed for the intrinsic GNR-FET using the quantum transport simulations described in Section 2. These values were used to populate a lookup table at discrete voltage steps of  $V_{GS}$  and  $V_{DS}$  ranging from 0V to 0.75V. The intrinsic gate and drain capacitances  $C_{GD,i}$  and  $C_{GS,i}$  vary with the gate and drain voltages. These values can be computed and stored in the lookup table by differentiating the channel charge w.r.t  $V_{GS}$  and  $V_{DS}$  respectively. Thus,  $C_{GD,i} = |\partial Q / \partial V_{DS}|$  and  $C_{G,i} = C_{GS,i} + C_{GD,i} = |\partial Q / \partial V_{GS}|$ , which yields  $C_{GS,i} = |\partial Q / \partial V_{GS}| - |\partial Q / \partial V_{DS}|$ .

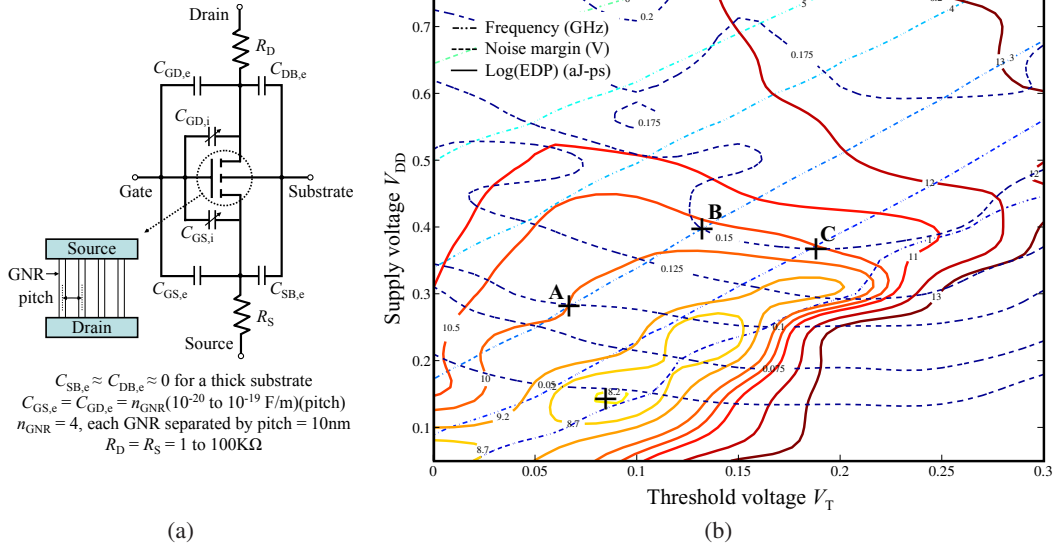


Figure 3: (a) Circuit model for GNRFET simulation (b) EDP, frequency, and SNM contours for a 15-stage ring oscillator

The extrinsic n-type and p-type GNRFETs were modeled by adding the parasitic capacitances and contact resistances around the intrinsic GNR as shown in Figure 2(a). Two strategies — fabricating very narrow contacts to an individual GNR or fabricating multiple GNRs in an array for a wide contact — are currently under investigation in the device community. The GNRFET considered in this paper is comprised of 4 equi-distant GNRs that form the channel. The pitch refers to the spacing between the neighboring GNRs in the GNRFET channel, and usually ranges from the GNR width to  $1\mu\text{m}$  as annotated in the figure. In this paper, we assume that an individual GNR channel has a contact width of 10nm, and that this equals the pitch in the GNR array. Thus, a GNRFET with 4 GNRs has a total contact width of 40nm. The current in the GNRFET is 4 times the current in the individual GNR channel, and the parasitics are also 4 times that for an individual GNR. Thus, the parasitic junction capacitances  $C_{GD,e}$  and  $C_{GS,e}$  are given by  $0.01\text{--}0.1\text{aF/nm}$  times the total GNRFET contact width of 40nm.

It is assumed that the substrate is thick enough that the extrinsic parasitic capacitances  $C_{DB,e}$  and  $C_{SB,e}$  are negligible. The contact resistances were assumed to range from  $1\text{K}\Omega$  to  $100\text{K}\Omega$ , with a nominal value of  $10\text{K}\Omega$ . The contact capacitance at the device terminals and interconnect capacitance are assumed negligible and are not considered in this paper.

### 3.1 Technology exploration

The trade-off between delay, energy, and noise robustness can be explored for different values of  $V_{DD}$  and  $V_T$  for GNRFET circuits. We choose a 15-stage ring oscillator where each inverter drives a fanout-of-four load as the representative circuit for this study. The energy-delay product (EDP) has been widely used to explore the tradeoffs between delay and power in CMOS circuits. The EDP captures how delay can be reduced by increasing  $V_{DD}$  and reducing  $V_T$ , dynamic power can be reduced by lowering  $V_{DD}$ , and static power can be reduced by increasing  $V_T$ . The EDP attains a minimum at an intermediate value of  $V_T$  and  $V_{DD}$ , and can be used for technology exploration of GNRFET circuits. Figure 2(b) presents the EDP contours (solid curves) for the ring oscillator. The optimum value of the EDP is achieved at  $V_{DD}=0.15\text{V}$  and  $V_T=0.08\text{V}$ , and is conventionally the preferred operating point for the circuit.

However, this optimum corresponds to a low frequency of operation. By plotting the frequency of operation that can be achieved

Table 1: Delay, EDP, and SNMs for GNRFETs and CMOS

Design Objective	Nominal GNRFET			Scaled CMOS ( $V_{DD}$ )								
	A	B	C	22nm		32nm		45nm				
	0.8V	0.6V	0.4V	0.8V	0.6V	0.4V	0.8V	0.6V	0.4V			
Freq. (GHz)	3.3	3.4	2.5	5.8	4.2	1.64	4.5	3.4	1.4	3.5	2.7	1.24
EDP. (fJ-ps)	22.7	27.6	36.8	1265	1129	1713	2688	2370	3259	5318	4645	6012
SNM (V)	0.09	0.14	0.15	0.3	0.23	0.16	0.31	0.24	0.16	0.32	0.25	0.17

for a 15-stage ring oscillator for each  $V_{DD}\text{-}V_T$  combination, it is possible to explore performance-energy tradeoffs further using the following observation. For a given desired frequency of operation, the optimum EDP curve is tangential to the frequency curve. For example, for a desired frequency of 3GHz for the 15-stage ring oscillator, point A in Fig. 2(b) suggests that the minimum EDP is attained at  $V_{DD}=0.3\text{V}$  and  $V_T=0.06\text{V}$ . However, this optimum point is always in the sub-threshold or low inversion region of operation, and poses challenges when noise immunity is considered as an additional figure-of-merit.

Reliability can be introduced as an additional figure-of-merit to determine optimum EDP for a desired frequency of operation by drawing the static noise margin (SNM) contours for an inverter. These contours represent points of equal SNM for each  $V_{DD}\text{-}V_T$  combination. Point A in the figure lies on the 0.1V SNM contour, which is unacceptable for most applications. When a desired SNM is identified, the intersection of the desired frequency and SNM contours identifies a region for reliable operation that achieves desired performance. The intersection of the two curves determines the point of minimum EDP. For example, for a SNM of 0.15V at 3GHz, the optimum  $V_{DD}\text{-}V_T$  combination is given by point B with  $V_{DD}=0.4\text{V}$  and  $V_T=0.13\text{V}$  in Fig. 2(b). This operating point offers a good trade-off between EDP, performance, and noise robustness.

Note that unlike CMOS, increasing  $V_T$  does not necessarily help tradeoff performance for higher noise robustness in GNRFET circuits. For example, the operating point C with  $V_{DD}=0.4\text{V}$  and  $V_T=0.23\text{V}$  has the same EDP and noise margins as point B in the figure. However, the frequency of the ring oscillator for operating point B is 40% greater than that for operating point C as seen in the figure. Higher  $V_T$  at C is achieved by decreasing the off-set as shown in Figure 2, which corresponds to operating the ring oscillator at a point other than that of minimum leakage as explained in Section 2. As a result, the resulting potential divider effect within the GNRFET inverter limits noise margins and decreases performance as observed in the figure.

**Comparison to scaled CMOS:** Table 1 compares the performance, EDP, and SNM of the 15-stage ring oscillator for GNR-FETs and scaled CMOS nodes (simulated using the PTM model [16]). For all scaled CMOS nodes,  $V_{DD} = 0.8V$  provides the best performance,  $V_{DD} = 0.4V$  consumes the least power, and  $V_{DD} = 0.6V$  has the optimum value of EDP.

A striking difference between the scaled CMOS nodes and GNR-FETs is that the optimum EDP for scaled CMOS is 40–168X higher than the EDP for GNR-FETs at operating point B. GNR-FETs have lower noise margins in comparison to scaled CMOS and are also more susceptible to variability and defects as discussed in the remainder of this paper. However, the significant difference in EDPs leaves enough headroom for robust design with GNR-FETs to overcome these challenges.

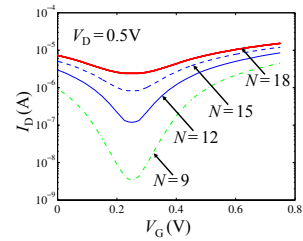
#### 4. Intrinsic GNR-FETs: Defects and variability

Variability and defects are expected to play an important role in graphene electronics in practice. Variability, for example, can come from the difficulty of control of the GNR width or oxide thickness in fabrication. The charge impurity in the gate insulator, lattice vacancy, or edge roughness [17] of GNR may be a defect which results in a large performance variation. Our atomistic NEGF simulation of a wide variety of variability and defect mechanisms have identified the important role of the GNR width variation and the effect of Coulomb charge impurities in graphene, which are the subject of this study. Other defect and variability mechanisms exist and should be explored in future studies, but we expect the effects are qualitatively similar and can be explored by readily extending the bottom-up simulation framework presented here.

The occurrence of variation and defect events in the GNR array channel of a GNR-FET is modeled and analyzed in two ways. In the first case, it is assumed that only one GNR in the array is subject to a variation, defect, or combination thereof. The total current is given by the sum of the currents in the GNRs, nominal or otherwise. Because the pitch is larger than the gate oxide thickness, an impurity near one GNR has a negligible effect on other GNRs because the impurity charge electric field is screened by the gate. In practice, multiple defects and variability of all GNRs in the array may exist and this is handled in the second case by assuming that each GNR in the channel experiences the same variation, defect, or combination thereof. The results in this work, therefore, establish lower and upper limits for the effects of variations and defects on GNR-FET circuits. Future studies are necessary to address multiple variability and defect effects, but we expect the broader conclusions to remain the same.

**GNR width variation:** The band-gap of the semiconducting GNR is, in general, inversely proportional to the GNR width. Because device characteristics are very sensitive to the band-gap of channel material, the width effect is critical to GNR-FET performance. GNR width is proportional to the GNR index. A-GNRs with an index of  $N=3q$  and  $N=(3q+1)$  are semiconducting GNRs and may be used as FET channels. Only GNRs with index values of 9, 12, 15, and 18 were selected to study the effect of variations in width in this paper. Starting with the minimum GNR index of  $N=9$ , which has a width of 1.1nm, the index is increased in steps of 3, or equivalently, by an incremental width of 3.7Å. Note that A-GNRs with an index of  $N=(3q+2)$  are semiconducting with a small band-gap and are not considered in this paper.

Figure 4 illustrates how variability in GNR width affects device  $I_D$ - $V_G$  characteristics. The band-gap of the  $N=18$  GNR is too small to achieve a small leakage current, whereas that of the  $N=9$  GNR is sufficiently large so that  $I_{on}/I_{off}$  is as high as 1000X. However, the



**Figure 4:  $I$ - $V$  characteristics for different GNR widths**

capacitance of a wider GNR-FET is large due to the larger surface of the GNR channel. The  $N=18$  GNR-FET has 50% larger intrinsic channel capacitance than the  $N=9$  GNR-FET in the on state, which can affect performance as discussed in the next section.

**Charge impurity:** A single charge impurity in the gate oxide makes an ideal device a more realistic device. For SBFETs, the charge impurity may affect device characteristics most severely when it is located close to the source because the Schottky barrier between source and GNR is affected. In our simulations, the charge impurity is considered as a fixed external charge in the gate oxide region, and it plays an important role for self-consistent electrostatic potential. To exaggerate the effects of an impurity, the impurity is placed near the source and at a distance of 0.4nm from the GNR surface. Both polarities of charges are considered, and the charge magnitude is also varied.

Figure 5(a) shows the severely affected Schottky barrier due to the charge impurity. The inset in the figure shows the position of the charge impurity in the cross-section of the simulated device. A negative charge impurity increases the barrier height and thickness, whereas a positive charge impurity decreases the barrier height and thickness at the source contact. This affects the source-drain current and the charge in the channel. With the negative charge impurity of  $-2q$ , the electron flow is significantly reduced by the large barrier, and the on current is a factor of 6 smaller than that in the ideal device. For the device with the  $+2q$  positive charge impurity, both off and on currents show a relatively smaller variation from the ideal device compared to that with the  $-2q$  negative charge impurity in the n-type operation branch ( $V_G > 0.25V$ ), as illustrated in Figure 5(b).

#### 5. GNR-FET circuits: Variations and defects

In this section we study the sensitivity of inverter delay, power, and noise robustness to variations in GNR width and charge impurities. The combined effect of variations in GNR width and charge impurities is also studied to identify the worst case combination of width variation and charge impurity on delay, power and noise margins. As explained in the previous section, two scenarios are considered: one where the anomaly affects one out of four GNRs in the array and the second where all four GNRs in the array are similarly affected. The simulations were performed for an inverter with a fanout-of-4 load. The operating point ( $V_{DD}=0.4V$  and  $V_T=0.13V$ ) derived in Sec. 3.1 as a good trade-off point between delay, energy, and noise robustness for the nominal device is used to simulate all the GNR-FET circuits in this section.

##### 5.1 Width variation

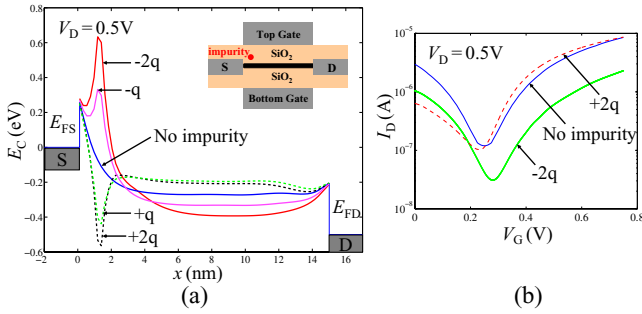
Table 2 shows the delay, power and, noise margin due to independent variations in GNR widths in both the n-type and p-type GNR-FETs of an inverter. The delay of an inverter driving a fanout-of-4 load, with nominal n-type and p-type GNR-FETs composed of four  $N=12$  GNRs in the array, is 7.54ps. The delay increases as the width of the GNR decreases to  $N=9$  and decreases as the width

**Table 2: Effect of independent variations in GNR width in n/p-GNRFET channels on inverter delay, power, and SNM**

	N	nGNRFET											
		Delay (%)				Static/Dynamic power (%)				SNM (%)			
		9	12	15	18	9	12	15	18	9	12	15	18
pGNRFET	9	6,77	3,37	0,26	-3,24	-13,-47/-8,-38	-6,-28/-4,-23	24,45/3,-10	92,248/11,4	0,15	-13,-33	-20,-67	<b>-27,-80</b>
	12	3,37	7.54 ps	-3,-9	-6,-15	-6,-28/-4,-23	0.095/0.706 $\mu$ W	32,95/7,24	201,338/17,47	-13,-33	0.15 V	-13,-40	-20,-62
	15	0,26	-3,-9	-6,-21	-9,-26	24,45/3,-10	32,95/7,24	65,305/15,56	238,468/26,84	-20,-67	-13,-40	-17,-23	-17,-46
	18	-3,24	-6,-15	-9,-26	-12,-30	92,248/11,4	201,338/17,47	238,468/26,84	<b>313,643/27,215</b>	<b>-27,-80</b>	-20,-62	-17,-46	-17,-41

**Table 3: Effect of independent charge impurities in n/p-GNRFET channels on inverter delay, power, and SNM**

Charge Impurity	pGNRFET	nGNRFET													
		Delay (%)					Static/Dynamic power (%)					SNM (%)			
		-2q	-q	0	+q	+2q	-2q	-q	0	+q	+2q	-2q	-q	0	+q
+2q	8,92	5,57	4,46	3,41	4,44	-9,-31/-9,-46	-8,-28/-7,-35	-5,-20/-5,-27	1,-7/-2,-22	-5,-24/-4,-26	-7,7	-7,-19	<b>-14,-40</b>	-13,-53	<b>-14,-40</b>
+q	5,57	3,23	1,12	1,7	2,10	-8,-28/-7,-35	-7,-22/-5,-22	-4,-12/-2,-12	2,4/0,-4	-4,-17/-2,-11	-7,-19	0,-6	-6,-13	-14,-27	-7,-27
0	4,46	1,12	7.54 ps	0,-5	0,-2	-5,-20/-2,-22	-4,-12/-2,-12	0.095/0.706 $\mu$ W	6,18/3,9	0,-5/0,0	<b>-14,-40</b>	-6,-13	0.15 V	0,-14	0,-7
-q	3,41	1,7	0,-5	-1,-9	0,-6	1,-7/-5,-27	2,4/0,-4	6,18/3,9	<b>11,37/5,19</b>	5,13/3,9	-13,-53	-14,-27	0,-14	0,-7	0,-13
-2q	4,44	2,10	0,-2	0,-6	1,-3	-5,-24/-4,-26	-4,-17/-2,-11	0,-5/0,0	5,13/3,9	-1,-10/0,0	<b>-14,-40</b>	-7,-27	0,-7	0,-13	0,-6



**Figure 5: (a) Conduction band profile of  $N=12$  GNRs with and without charge impurity. The inset shows the position of the charge impurity in the cross-section of the simulated device. (b)  $I$ - $V$  characteristics for  $N=12$  GNRs with charge impurities**

increases to  $N=18$ . In each entry in the table, the comma separates the first scenario when only one GNR is affected from the second scenario when all four GNRs in the GNRFET array are affected. In the worst-case, when one–four GNRs in both the p-type and n-type GNRFETs are  $N=9$  GNRs, the delay increases by 6–77%. On the other hand, there is a 12–30% decrease in the delay of an inverter when one–four GNRs in both the p-type and n-type GNRFETs are  $N=18$  GNRs. Variations in GNR width significantly impact both static and dynamic power. When one–four GNRs in both the p-type and n-type GNRFETs are  $N=9$  GNRs, static and dynamic power are reduced by 13–47% and 8–38% respectively. In the worst-case, however, static and dynamic power increase by 313–643% and 27–217% respectively. The impact of variations in width on leakage power stands out in this table, since even single GNR variations in the two GNRFETs can increase static power consumption by 3X. Finally, it is observed that GNR width variations affect the static noise margins of a GNRFET inverter significantly. When the n-type and p-type GNRFETs of an inverter have the same widths, the static noise margin increases with decrease in width due to the increase in inertial delay in the inverter. The noise margin decreases from 0.17V to 0.09V as the width (of both n-type and p-type GNRFETs) increases from  $N=9$  to  $N=18$ . However, the noise margins degrade further when n-type and p-type GNRFETs have different widths, and reach their worst-case deviations when there is maximum mismatch of  $N=9$  and  $N=18$  between the n-type and p-type GNRFETs. In this case, the static noise margin is off by 27–80% from its nominal value of 0.15V.

## 5.2 Charge impurities

Table 3 shows the delay, power, and noise margin due to independent charge impurities that affect one–four of the GNRs in both the n-type and p-type GNRFETs of an inverter. Note that a  $+q$  charge has the same effect on a pGNRFET device as a  $-q$  charge has on an nGNRFET device, and vice versa. The effect of charge impurities is highly asymmetric, with large degradation in delay, power, and noise margin and only small improvements. Inverter delay is degraded by 8–92% in the presence of simultaneous  $-2q$  and  $+2q$  charge impurities in one–four nGNRFETs and pGNRFETs respectively. However, the maximum improvement in delay observed due to the presence of simultaneous  $+q$  and  $-q$  charge impurities in one–four nGNRFETs and pGNRFETs respectively is 1–9%. Charge impurities affect static power more than dynamic power in a trend similar to that observed for variations, but to a smaller extent. When one–four GNRs in both the p-type and n-type GNRFETs are subject to  $+q$  and  $-q$  charge impurities respectively, static and dynamic power increase by 11–37% and 5–19% respectively. Charge impurity defects have a smaller effect on the noise margin of an inverter in comparison to variations in GNR width. The presence of simultaneous  $+q$  and  $-q$  charge impurities affecting one–four n-type and p-type GNRs respectively degrades the noise margin by 14–40%, with a 7% improvement in the best case.

## 5.3 Simultaneous defects and variations

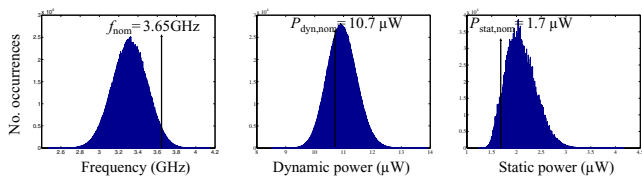
In this section, we study the worst-case impact of simultaneous variations in width ( $N=9/18$ ) and charge impurities ( $-q/+q$ ) on inverters and latches.

**Inverter:** The delay, power, and noise margins for simultaneous defects and variations in the GNRFET inverter are dominated by variations in GNR width and exacerbated by charge impurities. Thus, in the worst case when all GNRs in the array are affected, delay increases by over 2X, static power increases by over 7X, dynamic power increases by over 2X, and the noise margin reduces to zero. These effects are less pronounced on delay and noise margin when only one GNR in the array is affected. However, static power still increases by nearly 4X and dynamic power by 1.5X.

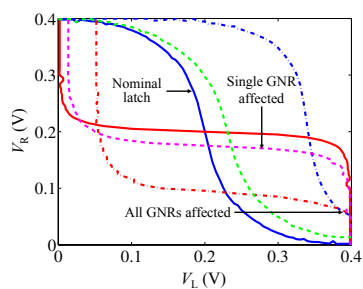
**Ring oscillator:** Monte Carlo simulations with independent variations in width ( $N=9/12/15$ ) and charge impurities ( $-q/0/+q$ ) of all inverters were run on the 15-stage ring oscillator. The width and charge impurities for the GNRFETs were drawn from a normal distribution, with mean width  $N=12$  and mean charge equal to zero.

**Table 4: Effect of independent variations and charge impurities in n/p-GNRFET channels on inverter delay, power, and SNM**

N,Charge		nGNRFET											
		Delay (%)				Static/Dynamic power (%)				SNM (%)			
		9,-q	9,+q	18,-q	18,+q	9,-q	9,+q	18,-q	18,+q	9,-q	9,+q	18,-q	18,+q
pGNRFET	9,+q	<b>6,142</b>	7,96	0,57	-4,53	85,-45/90,-52	88,-45/92,-40	161,62/105,-21	214,118/116,-12	0,21	-6,-13	-27,-87	<b>-34,-100</b>
	9,-q	7,96	8,50	0,12	-3,11	88,-45/92,-40	90,-42/93,-28	165,134/107,6	219,223/118,24	-6,-13	-7,8	-20,-67	-36,-87
	18,+q	0,57	0,12	-8,-24	-11,-28	161,62/105,-21	165,134	246,399/124,82	306,535/136,111	-27,-87	-20,-67	-7,-29	-28,-75
	18,-q	-4,53	-3,11	-11,-28	-14,-33	214,118/116,-12	219,223/118,24	<b>306,535/136,111</b>	371,684/149,142	<b>-34,-100</b>	-36,-87	-28,-75	-14,-81



**Figure 6: Monte Carlo simulations for 15-stage ring oscillator**



**Figure 7: SNM for latch with variations and defects**

The widths  $N=9/15$  and charge  $+q/-q$  were set to  $\sigma$  for the two distributions, which were discretized to reflect the nature of occurrence of variations and defects in GNRFETs. Figure 6 presents the distributions for delay, dynamic power, and static power for the oscillator. Although the mean value of dynamic power remains unchanged, the mean value of frequency decreases by 10% from the nominal value and the mean value of static power increases by 23% from the nominal value. This is expected because variations and defects cause more degradation than improvement in delay and static power (refer Table 4). These results illustrate that even at the optimum operating point, variations and defects have a significant impact on performance and static power in GNRFET circuits.

**Latches:** There is a lot of interest in using low power nanoelectronics to realize dense memory arrays. The tradeoffs involved are increased susceptibility to variations and defects, both of which impact the noise margins of memory cells and require high levels of error correction. Figure 7 shows butterfly curves for three cases: nominal, single GNR affected, and all GNRs affected. Both inverters in the latch are assumed to have the same widths and impurities. The worst case combination of defects and variations occurs when the nGNRFET has  $N=9$  and a  $+q$  charge impurity, and the pGNRFET has  $N=18$  and a  $-q$  charge impurity (or vice-versa, per Table 4). Due to the asymmetry in the n-type and p-type GNRFETs of the inverters in the latches, one eye of the butterfly curve collapses to reduce the noise margin to near-zero as shown in the figure. A second important observation is that the static power consumption of latches can increase by over 5X in the worst case ( $\approx$  the worst case for inverters), a source of concern for most memory applications. However, both the redundancy required for ECC as well as the high static power may be off-set by the advantages of high density and low power that GNRFETs offer over scaled CMOS.

## 6. Conclusions

Quantum effects and atomistic scale features inevitably play an important role in nanoscale electronic devices and circuits. We have developed a bottom-up multi-scale simulation framework that treats atomistic scale features in circuit simulations. The simulation framework is applied to technology exploration of GNRFET circuits, with an emphasis on variability and charge impurity effects. The GNR material promises ultra-small, fast, and low-energy FETs, but two key effects of variability and defects — leakage and low noise margins — are significant. For example, the variation of the channel width by a couple of Å changes the leakage current by orders of magnitude, and a single Coulomb charge impurity can lower the FET on-current by about 30%. Dense memories, which are the biggest prospect for graphene-based devices, are particularly susceptible to variations and defects with near-zero noise margins and an increase in leakage power of over 5X. This assessment of the effects of variability, defects, and parasitics indicate their important role on circuit performance. These effects must be carefully considered in the performance assessment and design optimization for future graphene-based electronics technology.

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