Transistor Sizing for Radiation Hardening

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Abstract

This paper presents an efficient and accurate numerical analysis technique to simulate single event upsets (SEUs) in logic circuits. Experimental results that show the method is accurate to within 10% of the results obtained using SPICE are provided. The proposed method is used to study the ability of a CMOS gate to tolerate SEUs as a function of injected charge and transistor sizing (aspect ratio $\frac{W}{L}$). A novel radiation hardening technique to calculate the minimum transistor size required to make a CMOS gate immune to SEUs is also presented. The results agree well with SPICE simulations, while allowing for very fast analysis. The technique can be easily integrated into design automation tools to harden sensitive portions of logic circuits.

1 Introduction

In the next decade, technology trends – smaller feature sizes, lower voltage levels, higher operating frequencies, reduced logic depth – are projected to cause an increase in the soft error failure rate in integrated circuits. While memories have historically been the focus for soft error failure rate reduction, recent studies indicate that the soft error failure rate in logic will increase to an extent where it will become comparable to present-day unprotected memory elements [Cohen 99], [Shivakumar 02]. As a result, there is an urgent need for techniques to estimate and reduce the soft error failure rate in logic circuits.

As the complexity of designs increase, the current practice of addressing the soft error robustness of a logic circuit following physical design will result in increased iterations in the design cycle. While SPICE -based characterizations of library cells after back-annotation are extensively used today, such techniques are inherently computationally expensive and incorporating them into logic synthesis engines and other design automation tools presents significant challenges.

There is a need for techniques to incorporate SEU-robustness metrics into the design cycle at higher levels of design abstraction, i.e., earlier in the design cycle, to realize inherently robust circuits. By working with a model that accurately captures the effects of a SEU for simulation purposes at the gate level, the computational bottleneck can be significantly alleviated. The purpose of this paper is to develop one such model for efficient and accurate analysis, and to show how that can be used to harden logic gates by transistor sizing. The following are the contributions of this paper:

1. An accurate model coupled with efficient numerical analysis to simulate SEUs in CMOS logic gates is presented. The transient voltage response is computed by solving the non-linear Riccati differential equation using the Runge-Kutta method.

2. The sizes of gates driving a node and the amount of capacitance at the node determine the magnitude and duration of the SEU transient. A novel transistor sizing method to harden a CMOS gate to SEUs is presented. This technique can be used with logic synthesis tools to identify and harden highly susceptible gates in a design, along the lines of the technique presented in [Mohanram 03].

The rest of this paper is organized as follows. In Section 2, we discuss previous literature and discuss the motivation for this paper in greater detail. In Section 3, we present the model and the numerical technique for SEU analysis. In Section 4, we discuss the effects of transistor sizing on SEU immunity and present an efficient technique to size transistors for radiation hardening in logic circuits. In Section 5, we present experimental results for the methods described in Sections 3 and 4. Section 6 is a conclusion.

2 Motivation and previous work

Several papers have addressed the problem of modeling and estimating the voltage transient that results at a logic gate following a SEU. An efficient and accurate

estimation of the rise time, the fall time, and the duration of the resulting transient voltage pulse is highly desirable. In [Dharchoudhury 94], the simulation time interval was divided into several independent segments (time intervals). A piecewise quadratic function (i.e., a quadratic function for each time segment) was used to approximate the double exponential waveform for the current pulse used to model a SEU at a node (Section 3, Equation 2). In [Dahlgren 95], although the current at the node where the particle strike occurs is modeled by a double exponential function, the contribution from the from the τ_β time constant (Section 3, Equation 2) was ignored. Other methods proposed in literature are mainly used for fault injection and simulation. There, accuracy is compromised for speed of computation, rendering them unsuitable for use in cases where accuracy is desirable.

In this paper we present a method to estimate the transient voltage waveform that is not just faster than traditional SPICE-based approaches but also highly accurate. Besides this, the other main motivation for this paper is the development of a fast transistor sizing method to eliminate the effects of a SEU at a logic gate by examining the relation between the transistor size and the injected charge. A large transistor can dissipate (sink) the injected charge as quickly as it is deposited, so that the transient does not achieve sufficient magnitude and duration to propagate to gates in the fanout. Moreover, since the voltage disturbance is a finite energy transient effect, the injected charge Q also needs to be factored in when selecting the optimal transistor size. There is a trade-off however, since increasing the transistor size will impact not just area but also power consumption and delay. The proposed technique can be used to balance overhead costs (area, power, delay) to choose the minimal transistor size to achieve the desired level of SEU immunity.

3 Modeling and analysis

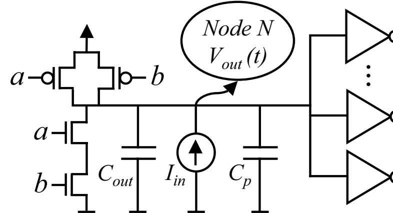

Figure 1: Example circuit

Figure 1 illustrates the CMOS circuit used to explain the modeling and analysis in this paper. C_{out} is the output capacitance at node N and is obtained by scaling the unit output capacitance C_{unit} by the transistor size $\frac{W}{L}$. C_p is the lumped parasitic capacitance (interconnect and fanout) at node N. The total capacitance associated with node N is given by

$$C_L = C_p + C_{unit}\left(\frac{W}{L}\right) \quad (1)$$

For the rest of this paper, we focus on the voltage $V_{out}(t)$ at node N, since its magnitude and duration will determine how the disturbance propagates through gates in its transitive fanout in the logic circuit to the primary outputs or latches.

$I_{in}(t)$ denotes the double exponential current pulse produced as a result of a particle strike at N. $I_{in}(t)$ has been approximated by a double exponential current pulse injected into the site of the particle strike [Messenger 82], [Dharchoudhury 94]:

$$I_{in}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}\left(e^{(-t/\tau_\alpha)} - e^{(-t/\tau_\beta)}\right) \quad (2)$$

In the above equation, Q is the amount of injected charge (positive or negative) that is deposited as a result of a particle strike, τ_α represents the collection time-constant of the junction, and τ_β accounts for the ion-track establishment time-constant. τ_α and τ_β are constants dependent on several process-related factors.

In this paper, we only consider the worse case transient effects to logic values 0 and 1. A transient to 1 (0) refers to the case when the steady-state logic value at N is 0 (1) in the fault-free case and a SEU generates a positive (negative) transition to 1 (0) at N. The rest of this section discusses the response of the NAND gate at node N when a SEU causes a transient to 1. The analysis for a SEU that causes a transient to 0 is symmetrical, with the use of pMOS transistor equations. Note that the pMOS transistors, whose inputs are at logic value 1, are off and hence do not figure in the analysis here. We set both inputs of the NAND gate to 1, so that the voltage is 0 at N in the fault-free case. For a transient to 1 in the NAND gate, the site for injection of current source $I_{in}(t)$ can be one of the internal nodes or the output of the gate. Since any disturbance internal to the gate has to propagate through one (or more) series transistors before reaching the output of the gate, the magnitude of the pulse will be reduced (or fade out altogether) during this propagation. Thus, the worst case occurs when the site for charge injection is the output of the gate (i.e., node N).

Note that the amplitude of the transient pulse at N given by $V_{out}(t)$ is limited by the forward bias voltage on the diode between the drain and the body of

the pMOS transistor. For a transient to 1, the drain to body diode that is reverse-biased under normal operating conditions may switch to forward-bias if the transient pulse rises above $V_{DD} + V_{diode}$. We focus on computing $V_{out}(t)$ in the 0 to $V_{DD} + V_{diode}$ range for the rest of this discussion.

Depending on the region of operation of the nMOS transistor, the voltage pulse $V_{out}(t)$ is given by the solution to the following differential equation:

$$C_L \frac{dV_{out}}{dt} = I_{in}(t) - \left(\frac{W}{L}\right) \cdot I_D(V_{out}) \quad (3)$$

where

$$I_D(V_{out}) = \beta \cdot (2(V_{GS} - V_{T,n})V_{out} - V_{out})^2 \quad (4)$$

for $V_{out} < (V_{DD} - V_{T,n})$ (linear) and

$$I_D(V_{out}) = \beta \cdot (V_{GS} - V_{T,n})^2 \quad (5)$$

for $(V_{DD} - V_{T,n}) \leq V_{out} < (V_{DD} + V_{diode})$ (saturation).

$V_{T,n}$ is the threshold voltage of the nMOS transistor, $I_{in}(t)$ is the injected current, V_{GS} equals V_{DD}, $\frac{W}{L}$ is the aspect ratio of the nMOS transistor, and C_L is the load capacitance at node N (as explained in Equation 1). The transconductance β is not a constant but a function of $V_{out}(t)$ and this has to be accounted for in the numerical analysis method presented in Section 3.1. A detailed explanation of how β is determined and approximated is presented in the appendix.

3.1 Numerical analysis for $V_{out}(t)$

Given the initial condition $V_{out}(0) = 0$, the above differential equation is a non-linear Riccati differential equation of the form

$$\frac{dV_{out}}{dt} = a(t) \cdot V_{out}^2 + b(t) \cdot V_{out} + c(t) \quad (6)$$

whose closed form solution usually requires knowledge of a particular solution [Kayssi 92]. Since a particular solution cannot be obtained in this case, the standard method of solving this differential equation is based on a power series expansion. An infinite power series solution for the transient response of an inverter, when no transient current of the form $I_{in}(t)$ is injected into the system, was proposed in [Shih 92]. Computation of the terms of an infinite power series is expensive in practice; moreover, it is very difficult to directly calculate the coefficient terms if more than a third order polynomial is used to approximate the solution.

We employ the fourth-order Runge-Kutta method [Nakamura 93] to calculate the numerical solution for Equation 3. The basic idea behind the Runge-Kutta method is that the value of the dependent variable, voltage $V_{out}(t)$ in this case, can be determined at the next desired value of the independent variable, time t, by calculating several intermediate values. Note that due to the parasitic and load capacitances at node N and the circuit inertia, the nature of the voltage waveform $V_{out}(t)$ is smooth and continuous. As a result, it is highly suitable for solution using the Runge-Kutta method. The fourth-order Runge-Kutta formulation is given by

$$V_{out}(t_{n+1}) = V_{out}(t_n) + \frac{h}{6}(k_1 + 2k_2 + 2k_3 + k_4) + O(h^5) \quad (7)$$

where h is the time step,

$f(t, V_{out}) = \frac{dV_{out}}{dt}$

$k_1 = f(t_n, V_{out}(t_n))$,

$k_2 = f(t_n + 0.5h, V_{out}(t_n) + 0.5k_1)$,

$k_3 = f(t_n + 0.5h, V_{out}(t_n) + 0.5k_2)$, and

$k_4 = f(t_n + h, V_{out}(t_n) + k_3)$

The solution for $V_{out}(t_{n+1})$ is accurate to the fourth order. In Section 5, we present results that show that the solution obtained using the proposed method is accurate to within 10% of the results obtained using Level 49 SPICE simulations.

4 Sizing for SEU immunity

In this section, we describe an efficient method to compute the minimum transistor size $\left(\frac{W}{L}\right)_{min}$ required to limit the maximum value of the transient pulse $V_{out}(t)$ at node N to a pre-specified value. We denote this limit on $V_{out}(t)$ by V_{SEU}. For the rest of this discussion, we assume this limit on the peak value V_{SEU} is $\frac{V_{DD}}{2}$ (that is V_{IH} for gates in the transitive fanout). Note that the method is equally applicable for any other limit on the peak value of $V_{out}(t)$. As $V_{out}(t)$ rises from 0 to $\frac{V_{DD}}{2}$, the nMOS transistor is in the linear region of operation. The cross-coupled nature of the differential Equation 3 implies that there is no closed form expression for the instant t_{max} when $V_{out}(t)$ reaches $\frac{V_{DD}}{2}$. However, since t_{max} occurs after the injected current $I_{in}(t)$ reaches its maximum, it is possible to use the following iterative procedure to compute t_{max}.

The first step is to determine a suitable search interval for t_{max}. The maximum value of $I_{in}(t)$ occurs at a

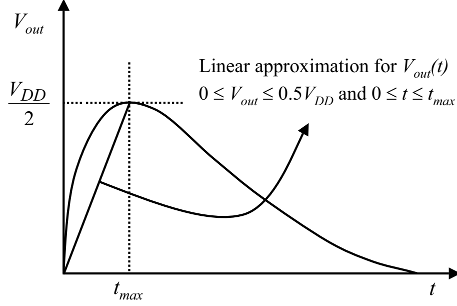

Figure 2: Linear approximation to compute $\left(\frac{W}{L}\right)_{min}$

time instant t_{start} that is given by

$$t_{start} = \left(\frac{\tau_\alpha \cdot \tau_\beta}{\tau_\alpha - \tau_\beta}\right) \cdot ln(\frac{\tau_\alpha}{\tau_\beta}) \tag{8}$$

from Equation 2. This can be used as the beginning of the search interval for t_{max}, since $t_{max} \geq t_{start}$. t_{max} is located in the interval $[t_{start}, t_{ref}]$, where t_{ref} is bounded by the clock period of the logic circuit.

If $\frac{V_{DD}}{2}$ is the maximum value of $V_{out}(t)$ at time t_{max}, two conditions must be satisfied by Equation 3. The first is that the slope $\frac{dV_{out}}{dt}$ must equal 0, i.e.,

$$I_{in}(t_{max}) - \left(\frac{W}{L}\right) I_D \left(\frac{V_{DD}}{2}\right) \; = \; 0 \tag{9}$$

Rearranging this, we have

$$\left(\frac{W}{L}\right)_{min} = \frac{I_{in}(t_{max})}{I_D(\frac{V_{DD}}{2})} \tag{10}$$

where $\left(\frac{W}{L}\right)_{min}$ is the minimum transistor size required to limit the magnitude of the transient pulse at node N to $\frac{V_{DD}}{2}$. The second condition is that the integral of both sides of Equation 3 over the interval $[0, t_{max}]$ must be equal, i.e.,

$$\begin{aligned}(C_{unit} \cdot \left(\frac{W}{L}\right)_{min} + C_p) \int_0^{\frac{V_{DD}}{2}} \left(\frac{dV_{out}}{dt}\right) dt = \\ \int_0^{t_{max}} I_{in}(t)dt - \left(\frac{W}{L}\right)_{min} \cdot \int_0^{t_{max}} I_D(V_{out})dt\end{aligned} \tag{11}$$

Since $I_D(V_{out})$ is a non-linear equation that depends on $V_{out}(t)$, we use the following approximation to simplify the integration. We assume that the voltage $V_{out}(t)$ rises from 0 to the peak value of $\frac{V_{DD}}{2}$ linearly as shown in Figure 2, i.e.,

$$V_{out}(t) = \left(\frac{V_{DD}}{2}\right) \cdot \left(\frac{t}{t_{max}}\right) \text{ for } 0 \leq t \leq t_{max} \tag{12}$$

As a result, I_D is just a function of time t and Equation 11 is directly integrated to get a non-linear equation in $\left(\frac{W}{L}\right)_{min}$ and t_{max}. This, along with Equation 10, can be solved using the bisection method [Nakamura 93] over the interval $[t_{start}, t_{ref}]$ to determine both unknowns t_{max} and $\left(\frac{W}{L}\right)_{min}$. In Section 5, we present experimental results that use this method to determine $\left(\frac{W}{L}\right)_{min}$ that are in excellent agreement with those obtained using SPICE.

5 Experimental results

The SPICE library used for all simulation is the TSMC 0.18 micro library distributed by [MOSIS]. The transconductance parameter β, for a range of transistor sizes, is an input from SPICE to the proposed setup (as explained in the appendix). The unit output capacitance C_{unit} was also determined using SPICE and scaled according to Equation 1. We used $\tau_\alpha = 0.2$ns and $\tau_\beta = 0.05$ns in all our experiments.

5.1 Calculation of $V_{out}(t)$

In Figure 3, we present a comparison between three sets of curves for $V_{out}(t)$. Each set of curves corresponds to different amounts of charge injected (i.e., SEUs of different strengths) as annotated in the figure. The transistor size remained fixed in all the cases. The solid curve in each set was obtained using the numerical analysis method described in Section 3.1, while the dashed curve was obtained from SPICE simulations. It is clear that for fixed transistor sizing, SEUs of greater magnitude produce transients of larger swing and duration at the output of the gate in comparison to SEUs of smaller magnitude. It is also clear that the proposed numerical analysis technique is very accurate and that the results vary by less than 10% from those obtained by Level 49 SPICE simulations.

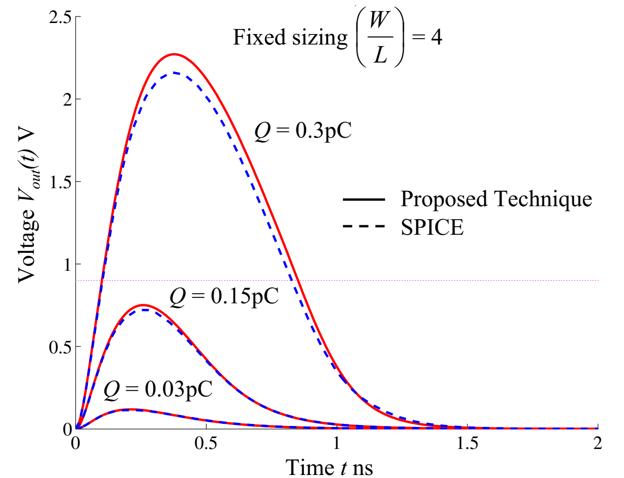

Figure 3: $V_{out}(t)$ for varying charge and fixed $\frac{W}{L}$

In Figure 4, we present a similar comparison between three sets of curves for $V_{out}(t)$. The only change from Figure 3 is that the three sets of curves correspond to different aspect ratios (different $\frac{W}{L}$s) for the nMOS transistors, while the total injected charge (i.e., the magnitude of the SEU) remains constant. It is clear that for fixed SEU magnitude, increasing the transistor size has the desired effect of reducing the magnitude and duration of the transient voltage pulse at the output of the gate.

In Figure 5, we varied the width of the transistor continuously for three different values of charge injected into the node N. The pulse width of the transient, given by the time that $V_{out}(t)$ exceeds $\frac{V_{DD}}{2}$ was measured for each of the cases. It is clear that there is an excellent agreement between the results obtained using proposed numerical analysis method and those obtained using SPICE simulations. It is also clear that as the transistor size increases, the magnitude and duration of the transient voltage pulse (as measured about $\frac{V_{DD}}{2}$) decreases and for large enough sizing, becomes zero. This observation can be exploited to radiation harden gates by sizing transistors, as described in the next section.

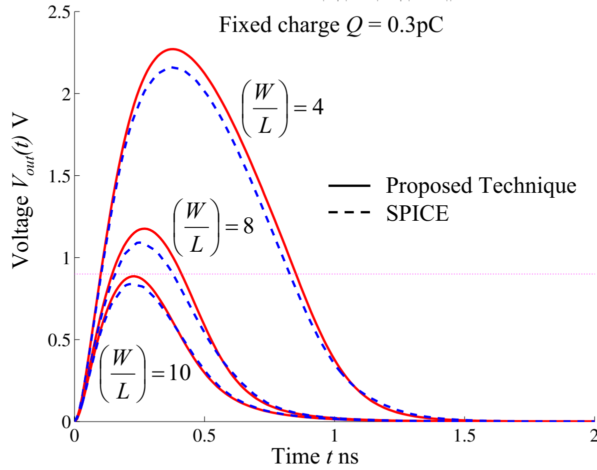

Figure 4: $V_{out}(t)$ for varying width and fixed charge

Note that for $Q = 0.4pC$ and $\frac{W}{L} = 4$, the magnitude of the transient pulse exceeds $V_{DD} + V_{diode}$ significantly when the proposed model is used. While this is a limitation of the model, it is not in the region of interest as far as the transient response is concerned because of its severe nature.

5.2 Sizing for SEU immunity

In Figure 6, we present the minimum transistor aspect ratio $\frac{W}{L}$ needed to limit the peak of the voltage transient to $\frac{V_{DD}}{2}$ for different values of injected charge. The solid curve represents the results obtained using the method proposed in Section 4 while the dotted curve represents the results obtained from SPICE. It is clear from the figure that the proposed method, whose results are in excellent agreement to those obtained using SPICE, has the twin advantages of accuracy and computational efficiency. The number of iterations to determine $\left(\frac{W}{L}\right)_{min}$ using the bisection method for an error tolerance of 0.001ns and $t_{ref} = 1$ns is 7. The routines were implemented in C and can easily be integrated into a logic synthesis tool that sizes transistors for radiation hardening.

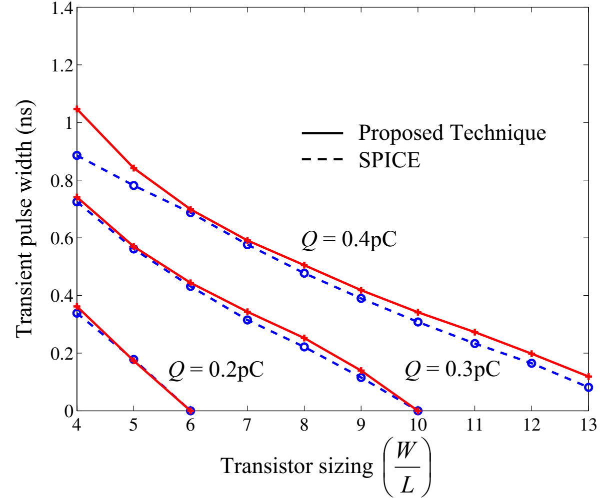

Figure 5: Transient pulse width vs. $\left(\frac{W}{L}\right)$

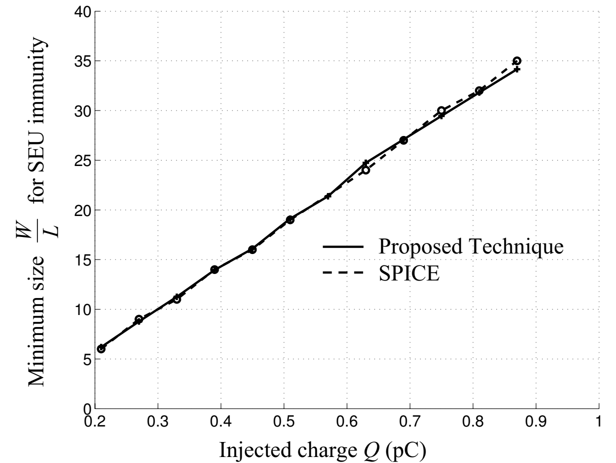

Figure 6: Sizing for SEU immunity

6 Conclusions

In the future, as designs become more complex and as the soft error failure rate of logic circuits becomes unacceptably high, there will be a need for simulation and design automation techniques for radiation hardening. This paper described an efficient and accurate technique to simulate SEU effects in logic gates. A novel technique for transistor sizing to reduce SEU susceptibility that is very accurate in comparison to SPICE was also described. An area for future research is to investigate how this sizing technique can be used to selectively target the most sensitive nodes in a logic circuit.

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Appendix

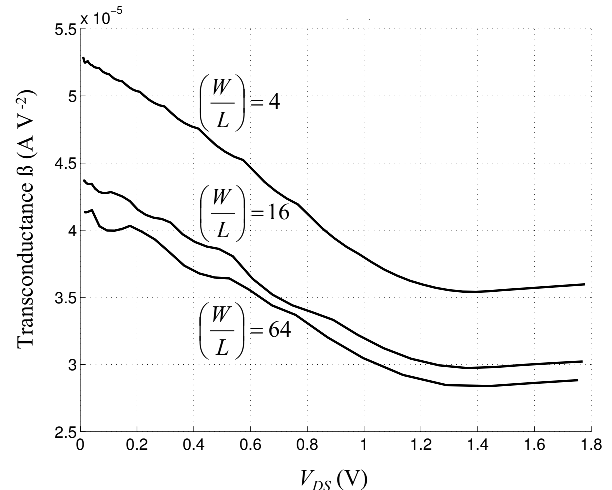

Figure 7: Transconductance $\beta(V_{DS})$ for a NAND gate

The transconductance β of a NAND gate is not constant but varies significantly with V_{DS} and to a small extent with the transistor size $\frac{W}{L}$. We remove the dependence on $\frac{W}{L}$ by averaging over the three curves shown in Figure 7. We define two linear functions to model the dependence of β on V_{DS}, one for the region $0 \leq V_{DS} \leq 1.2$ V and the second for values of $V_{DS} > 1.2$ V. This is an empirical model that is used in Equation 3 in the paper.