

# Parameter-Variation-Aware Analysis for Noise Robustness

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## Abstract

This paper studies the impact of variability on the noise robustness of logic gates using noise rejection curves (NRCs). NRCs allow noise pulses to be modeled using magnitude-duration profiles, and can be used to derive a noise susceptibility metric for the noise robustness of logic gates. Analytical methods — based upon calibration runs in circuit simulators — to determine noise susceptibility in the presence of variations in process, design, and environmental parameters ( $L_{\text{eff}}$ ,  $V_T$ ,  $V_{\text{DD}}$ , and  $W$ ) are described. Such analytical methods can be used not only to accurately estimate the impact of variability on noise robustness, but also to optimize designs for noise robustness.

## 1. Introduction

It is widely acknowledged that variations in parameters will pose a significant challenge to aggressive technology scaling into the sub-100nm regime [1]. Parameter variability can be categorized into process variability (e.g., effective channel length  $L_{\text{eff}}$ , threshold voltage  $V_T$ ), environmental variability (e.g., supply voltage  $V_{\text{DD}}$ , temperature), and variability due to device fatigue phenomena (e.g., hot electron effects, negative-bias temperature instability) [2]. Variability in delay, power, and yield due to these factors and statistical optimization techniques that maximize these design objectives in the presence of variability has been the subject of extensive research in both academia and industry (e.g., [3, 4]).

These advances notwithstanding, the impact of variability on the noise robustness of logic gates remains as such an unexplored area of research. For example, parameter variations can impact the noise robustness of a gate by increasing its vulnerability to crosstalk, by decreasing its ability to recover from charge collection due to particle strikes, and by increasing its ability to propagate transient pulses unattenuated [5, 6]. To the best of our knowledge, this is the first paper that studies and models the impact of variability on the noise robustness of logic gates.

It is possible to use static noise margin (SNM) as a figure-of-merit to measure the noise robustness of logic gates. Indeed, this is the approach taken in [7] to study and analytically predict the impact of  $V_T$  variations on the read and write stability of SRAM cells. SNM is an effective metric for SRAM cells because of the large read access time associated with SRAMs. However, SNM can be overly pessimistic for transients that are usually associated with noise. To avoid the pessimism introduced by SNMs, this paper uses noise rejection curves (NRCs) [8] that allow noise pulses to be modeled using magnitude-duration profiles to propose a noise susceptibility metric for logic gates.

Based upon this metric, Monte Carlo simulations show that variations in the process parameters  $L_{\text{eff}}$  and  $V_T$  have significant impact on noise robustness of designs. Analytical methods — based

upon calibration runs in circuit simulators — to estimate NRCs and noise susceptibility in the presence of variations in process, design, and environmental parameters ( $L_{\text{eff}}$ ,  $V_T$ ,  $W$ ,  $V_{\text{DD}}$ ) are then described. In all cases, the NRCs in the presence of variations are derived from base curves obtained during the calibration runs. Such analytical expressions for noise susceptibility can be used not only to estimate the impact of variations in process and environmental parameters, but also to statistically optimize designs for noise robustness. Such techniques are advantageous over simulation-based estimation and optimization for noise robustness that may be prohibitively expensive for larger circuits.

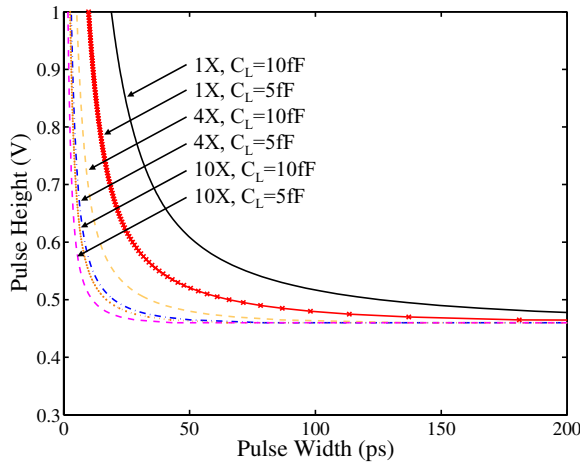
This paper is organized as follows. Section 2 introduces NRCs and the noise susceptibility metric. Section 3 discusses the impact of process variations in  $L_{\text{eff}}$  and  $V_T$  on noise robustness. Section 4 presents analytical methods to predict NRCs and noise susceptibility in the presence of variability. Section 5 concludes the paper and describes directions for future research.

## 2. Noise rejection curves

A standard figure-of-merit for the noise immunity of logic gates is based upon the static noise margin (SNM) of the gate. However, SNM can be pessimistic for noise pulses of very small duration since it does not consider the fact that logic gates act as low pass filters. In other words, since input pulses of small duration have more high frequency components than input pulses of large duration, a narrow input pulse may not propagate through the gate even if its magnitude exceeds the SNM of the gate. Whereas SNM may be a good measure for noise immunity on SRAM data reads where cycle time is generally long, it is a poor, pessimistic measure for noise immunity of noise pulses that affect logic gates.

A noise pulse can be characterized by its magnitude (denoted by  $H$  throughout this paper) and duration (denoted by  $\Delta$ ). When a noise pulse is applied at the input of a gate, the gate is said to reach the point of instability if (i) the gate inputs permit the propagation of the pulse to the output, i.e., they sensitize the gate, (ii)  $H$  is greater than the SNM, and (iii)  $\Delta$  exceeds a critical value,  $\Delta_c$ . Instability is defined with respect to a preset value,  $\eta V_{\text{DD}}$  ( $0 < \eta < 1$ ), by which the output of the affected gate must deviate from its steady-state value. In general,  $\eta$  is 10–40%. In this paper,  $\eta$  was set to 25%. Consider a gate with a steady-state output of  $V_{\text{DD}}$  subjected to a noise pulse at its input that causes the output voltage to decrease. If the magnitude of the input pulse exceeds the SNM of the gate, its output will fall for the duration of the noise pulse, before eventually being restored to its steady-state value. When the output reaches the critical voltage  $V_c = (V_{\text{DD}} - \eta V_{\text{DD}})$ , the gate is said to be unstable.

Noise rejection curves (NRCs) factor in such magnitude versus critical duration profiles for noise pulses. NRCs are illustrated for



**Figure 1: Noise rejection curves for an inverter. Larger size and smaller load capacitance increase noise susceptibility,  $\psi$ .**

an inverter in Figure 1. For a given load capacitance at the output of the gate, NRCs represent the magnitude-duration combination that is required at the input to drive the gate to the point of instability. The NRC shows that even if the pulse magnitude exceeds the SNM, the pulse will not result in instability if the pulse duration is not large enough. Therefore, NRCs provide a better estimate for the noise immunity of a gate. In the figure, the region below the NRC represents the “safe zone” of operation. As the gate size increases, or the load capacitance decreases, the gate becomes more susceptible to noise and the curves shift downward reducing the area of the “safe zone” under the NRC.

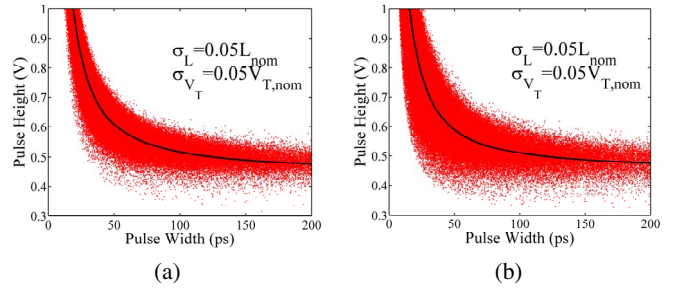
Integrating metrics for noise robustness into circuit optimization flows that focus on delay and power can decrease the probability of functional failures due to noise, and thereby increase design reliability. Although an NRC provides more information than SNM for a gate, it is necessary to abstract this into a single metric that can be integrated into optimization flows. We propose a new metric — noise susceptibility, denoted by  $\psi$  — that is given by the area above the NRC up to a maximum pulse duration,  $\Delta_{\max}$ . The value for  $\Delta_{\max}$  may be chosen based on (i) the frequency of operation or (ii) the pulse width required to destabilize, say, a minimum-sized inverter with the largest load capacitance. Since NRCs represent pulse height  $H$  as function of the pulse duration  $\Delta$ , noise susceptibility is given by:

$$\psi = \int_0^{\Delta_{\max}} (V_{DD} - H(\Delta)) d\Delta \quad (1)$$

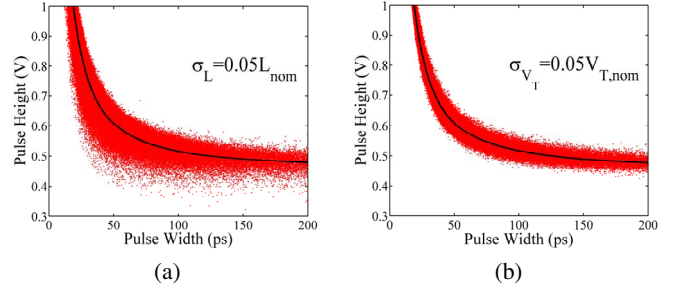
From Figure 1, it is clear that as gate size increases, the noise susceptibility  $\psi$  increases. This trend is opposite to gate delay, which decreases with increasing gate size.

### 3. Parameter variations and NRCs

This section presents and discusses simulation results for the effect of parameter variations on the NRCs of logic gates. The circuits were designed using the predictive technology models for the 65nm technology node [9]. Simulations were performed using a SPICE-based Monte Carlo framework where the parameters were considered to be independent Gaussian random variables with standard deviation equal to 5% of the mean value, i.e.,  $\sigma = 0.05\mu$ . Variations in the effective channel length,  $L_{\text{eff}}$ , and threshold voltage,  $V_T$ , of a minimum size inverter are considered. Since device



**Figure 2: Effect of variations in the parameters  $L_{\text{eff}}$  and  $V_T$  on the NRC of an inverter for (a) rising and (b) falling input noise pulse.**

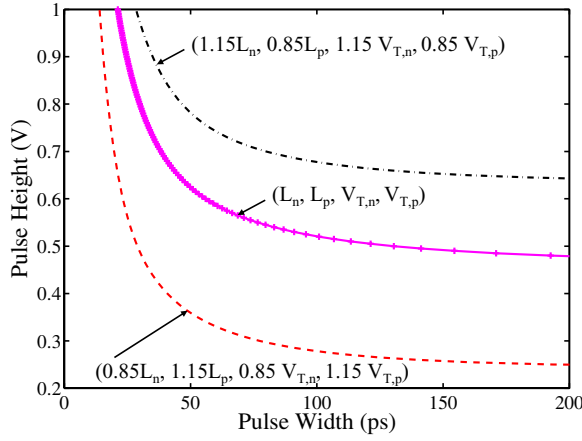


**Figure 3: Effect of variation of the parameter (a)  $L_{\text{eff}}$  and (b)  $V_T$  on the NRC of an inverter.**

mismatches make the circuit more vulnerable to noise,  $L_{\text{eff}}$  and  $V_T$  of the transistors in the pull-up and pull-down paths were varied independently. Variations in design and environmental parameters  $V_{DD}$  and gate size  $W$  were ignored in these simulations. However, they are accounted for in the analytical derivations presented in the next section.

The combined effect of parameter variations in  $L_{\text{eff}}$  and  $V_T$  on the NRC of the inverter is shown in Figure 2(a). The steady-state value of the inverter is  $V_{DD}$  before noise pulses are applied at its input. The nominal curve with no parameter variations is given by the solid line in the figure. It can be seen that for a given pulse duration, noise pulses of height much smaller than the height given in the nominal NRC can destabilize the gate. For example, for a pulse width of 25ps, the required pulse duration to destabilize the gate is 0.9V on the nominal NRC. However, when parameter variations are taken into consideration, a 0.58V pulse can result in noise instability. These simulations illustrate how parameter variations can severely affect the noise susceptibility of logic gates. Figure 2(b) shows the results when the steady-state output of the inverter is at voltage ground for derivation of the NRC. It is clear that the NRCs are similar when gates are subject to noise pulses with rising or falling profiles. Without loss of generality, the discussion for the rest of this paper focuses on noise pulses that perturb gates from a steady-state value of  $V_{DD}$ .

To evaluate the relative importance of variations in  $L_{\text{eff}}$  and  $V_T$ , they were varied individually with the other parameter at the nominal value. Results of these simulations are presented in Figures 3(a) and 3(b). From the figure, it is clear that variations in  $L_{\text{eff}}$  have a higher impact on the noise susceptibility of a gate in comparison to  $V_T$ . Regardless, variations in both process parameters have signifi-



**Figure 4: Noise rejection curves of an inverter for corner cases of  $L_{\text{eff}}$  and  $V_T$  variations. The parameters of the pMOS and nMOS transistors are varied separately.**

cant impact that must be factored into design.

Corner-based analysis can be used to illustrate how worst-case variations in the parameters of the pMOS and nMOS transistors can affect the noise susceptibility of logic gates. Figure 4 illustrates the best and worst NRCs for independent variations in the  $L_{\text{eff}}$  and  $V_T$  of the nMOS and pMOS transistors of an inverter. For a rising noise pulse at its input, when its steady-state output is at  $V_{\text{DD}}$ , the inverter is most susceptible to noise when the gate length  $L_n$  and threshold voltage  $V_{T,n}$  of the nMOS transistor are the minimum and when  $L_p$  and  $V_{T,p}$  are the maximum for the pMOS transistor. This is to be expected, since the pull-down path is much stronger than the pull-up path. This causes the output voltage to fall faster, and the weak pull-up path is relatively ineffective in restoring the output to its steady-state value. Similarly, when  $L_p$  and  $V_{T,p}$  of the pMOS are at the minimum and  $L_n$  and  $V_{T,n}$  of the nMOS are at the maximum, the pull-up path is much stronger than the pull-down path. This is the case when the gate is most robust to noise, as shown by the upward shift of the nominal NRC in the figure.

#### 4. Analytical derivation of NRC

Although it is possible to use corner-based analysis to comprehend the best and worst case scenarios for the noise susceptibility metric  $\psi$ , this can lead to conservative design. This section presents techniques for analytical prediction of gate NRCs for different combinations of parameter values. Analytical derivation of the NRC enables efficient design optimization through the noise susceptibility metric,  $\psi$ . This is advantageous over corner-based analysis and design, and can be used to replace circuit simulators that are computationally expensive and ineffective for use in circuit optimization. Just as the alpha power law and logical-effort-based expressions for delay and power enable efficient delay-power optimization in digital circuits, analytical expressions for  $\psi$  will facilitate the inclusion of noise robustness as an additional metric into such flows.

It is possible to model the pull-up and pull-down networks of any CMOS logic gate by an equivalent pull-up resistance, a pull-down resistance, and an output capacitance. Each of the three elements can be modeled as a function of the input and the output voltage. Since the region of operation of the transistors in the gate varies continuously, the effective resistances of the pull-up and pull-down

paths are non-linear functions of the operating point. Although the pull-up and pull-down resistances can be modeled independently, they are modeled by an equivalent resistance  $R_{\text{eq}}$  in this paper. The rest of this section describes how SPICE-based calibration runs can be used to analytically derive the NRC as a function of process parameters  $L_{\text{eff}}$  and  $V_T$  as well as design parameters  $V_{\text{DD}}$  and  $W$ . Variability in these parameters, and the effect on the NRC is considered in all cases.

Let  $C_{\text{eq}}$  be the effective output capacitance at the output of the gate. The solution of the first-order differential equation using the equivalent RC model for the gate is given by

$$V(t) = V_f + (V_{\text{DD}} - V_f) \exp\left(-\frac{t}{R_{\text{eq}}C_{\text{eq}}}\right) \quad (2)$$

where  $V_f$  is the voltage that the output will stabilize at for large  $\Delta$ . At the critical pulse duration  $\Delta_c$ , as defined in Section 2, the output reaches the critical voltage:  $V(\Delta_c) = V_c$ .

When the gate length, threshold voltage, gate size or the  $V_{\text{DD}}$  change, the values of  $V_c$ ,  $V_f$ ,  $R_{\text{eq}}$  and  $C_{\text{eq}}$  change correspondingly, thereby producing a shift in the NRC. We denote the points on the noise rejection curve of the base gate by the pulse height-width pairs,  $\{(H_1, \Delta_1), (H_2, \Delta_2), \dots, (H_n, \Delta_n)\}$ , and the corresponding points on the NRC of the gate with parameter variations by  $\{(H'_1, \Delta'_1), (H'_2, \Delta'_2), \dots, (H'_n, \Delta'_n)\}$ . Consider an arbitrary pulse  $\{H, \Delta\}$ . If the base case is denoted by using the subscript 'base' in Equation (2), the pulse width  $\Delta$  is given by:

$$\Delta = R_{\text{eq,base}}C_{\text{eq,base}} \ln\left(\frac{V_{\text{DD,base}} - V_f, \text{base}}{V_c, \text{base} - V_f, \text{base}}\right) \quad (3)$$

With parameter variations, the pulse shifts to  $\{H', \Delta'\}$  where  $\Delta'$  is given by:

$$\Delta' = R_{\text{eq}}C_{\text{eq}} \ln\left(\frac{V_{\text{DD}} - V_f}{V_c - V_f}\right) \quad (4)$$

Combining Equations (3) and (4) gives:

$$\Delta' = \Delta \frac{R_{\text{eq}}C_{\text{eq}}}{R_{\text{eq,base}}C_{\text{eq,base}}} \frac{\ln\left(\frac{V_{\text{DD}} - V_f}{V_c - V_f}\right)}{\ln\left(\frac{V_{\text{DD,base}} - V_f, \text{base}}{V_c, \text{base} - V_f, \text{base}}\right)} \quad (5)$$

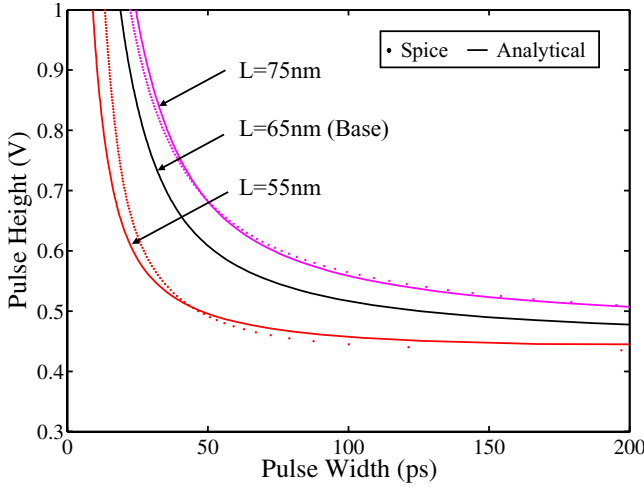
Using Equation 5, the NRC can be predicted for cases different from the base case. In the following section, we will investigate the impact of the variation of gate length,  $L$ , threshold voltage,  $V_T$ , gate size,  $W$ , and the supply voltage  $V_{\text{DD}}$ . However, since the variations of  $V_T$  and  $V_{\text{DD}}$  interact closely with each other, they are considered together. Note that once the curves are generated using circuit simulators and calibrated, only the base NRC curve is necessary to generate the NRCs in the presence of variability.

##### 4.1 Effect of gate length variation

When the gate length is changed from the base length  $L_{\text{base}}$  to any length  $L$ ,  $V_f$  remains almost the same since the resistances of the pull-up and pull-down paths change proportionately. The total capacitance given by the sum of the drain and load capacitances also changes minimally since a change in gate length does not significantly alter the overlap capacitances ( $C_{\text{eq}} = C_{\text{eq,base}}$ ). Only the resistance varies non-linearly with the gate length, and simulation results indicate that the following power law captures the change in equivalent resistance with the gate length:

$$\frac{R_{\text{eq}}}{R_{\text{eq,base}}} = \left(\frac{L}{L_{\text{base}}}\right)^\gamma \quad (6)$$

where  $\gamma$  is 1.5 for the longest gate, 4.0 for the shortest gate and linearly approximated for gate lengths in between.



**Figure 5: Comparison of the predicted and simulated NRCs for extreme gate lengths.**

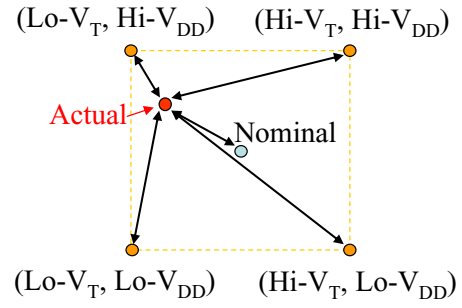
Using the above equation, the the NRCs for gates of different lengths were predicted using the base NRC for  $L = 65\text{nm}$ , as shown in Figure 5. Gate lengths over the range  $55\text{nm}$  to  $75\text{nm}$  (for  $3\sigma$  variation of 15%) were considered in these simulations. The SPICE simulation results are shown by dotted curves and the predicted curves by solid lines. The figure show that the predicted curves are in good agreement with the simulated curves. As seen in the figure, an increase in gate length makes the gates more robust to noise. The increase in gate length can effectively be thought of as “scaling up” the technology, and this enhances the robustness to noise.

## 4.2 Effect of $V_T$ and $V_{DD}$ variations

Threshold voltage,  $V_T$  and supply voltage,  $V_{DD}$ , have great impact on the noise robustness of a gate since the critical pulse height for a given pulse width strongly depends on these quantities. Therefore, the accuracy of the NRCs will strongly depend on how accurately the effect of  $V_T$  and  $V_{DD}$  variation is modeled. Variations in  $V_T$  and  $V_{DD}$  change the operating region of the devices, and this affects the accuracy of the scaling of the pull-up and pull-down resistance. This is because the pull-up and pull-down resistances are functions of the input and output voltage, which has implicit dependency on  $V_T$  and  $V_{DD}$ .

Simulations indicate that due to the high non-linear dependence of the resistances on  $V_T$  and  $V_{DD}$ , there is considerable error in predicting the NRCs from a single base curve. When  $(V_{DD} - V_T)$  is large, the resistance values can be derived from a single base case with minimum error. However, when  $(V_{DD} - V_T)$  is small, there is significant mismatch between the actual and predicted NRCs. This is solved by adopting a 4-corner method that calibrates for the  $(lo-V_{DD}, lo-V_T)$ ,  $(lo-V_{DD}, hi-V_T)$ ,  $(hi-V_{DD}, lo-V_T)$  and  $(hi-V_{DD}, hi-V_T)$  cases, as shown in Figure 6. Depending on the distance of the case under consideration from the corners and the nominal case, the base curve used for prediction is selected.

For variations in  $V_T$  and  $V_{DD}$ , it is essential to determine the resistance at the changed operating point for use of Equation 5. Because of the change in both  $V_{DD}$  and  $V_T$ , the average input voltage ( $V_{GS}$ ) and the gate overdrive voltage ( $V_{GS} - V_T$ ) change accordingly. Simulations indicate that an alpha-power law given by the



**Figure 6: Corners in the  $V_{DD}$ - $V_T$  space for determining the NRCs with variations in  $V_{DD}$  and  $V_T$ .**

expression below approximates the scaling of the resistance:

$$\frac{R_{eq}}{R_{eq,base}} = \left( \frac{V_{GS,base} - V_{T,base}}{V_{GS} - V_T} \right)^\alpha \quad (7)$$

where  $V_{GS,base}$  and  $V_{GS}$  are the average input voltage for the base and altered case and  $\alpha$  is 1.2 for the cases shown in Figure 7. As shown in the figure, there is negligible error between the predicted and simulated NRCs in all four cases.

## 4.3 Effect of gate sizing

When the size of the gate is changed from the base size  $W_{base}$  to any size  $W$ , the values of  $V_f$  and  $V_c$  remain the same since the pull-up and pull-down resistors scale down identically. However, the equivalent output resistance and capacitance change with the width as:

$$\frac{R_{eq}}{R_{eq,base}} = \frac{W_{base}}{W} \quad (8)$$

$$\frac{C_{eq}}{C_{eq,base}} = \frac{C_L + WC_d}{C_L + W_{base}C_d} \quad (9)$$

where  $C_L$  is the load capacitance and  $C_d$  is the drain capacitance of a unit sized gate. Using Equation 5, we can express the relation between  $\Delta'$  and  $\Delta$  by the following equation:

$$\Delta' = \frac{R_{eq}C_{eq}}{R_{eq,base}C_{eq,base}} \Delta \quad (10)$$

From the relation between  $\Delta'$  and  $\Delta$ , we can see that the pulse widths depend on the gate size in a manner that is analogous to the dependence of delay on logical effort [10]. The comparison in this case is made using the required pulse width to produce the same output noise with the same input voltage as the reference.

Figure 8 shows the results derived from the base NRC of a 1X inverter with 10fF load capacitance. From the base NRC, the NRCs are predicted for inverters of different sizes and load capacitances. The original NRCs are derived from SPICE simulations and are in excellent agreement with the predicted curves for all the cases considered in the figure.

## 4.4 Computation of $\psi$

The noise susceptibility metric can be computed from the NRCs predicted in Sections 4.1- 4.3. Let the base NRC have  $n$  points corresponding to pulse heights  $H_i = V_{min} + (i - 1)h$ , where  $V_{min}$  is the minimum pulse height that can produce a minimum perturbation of  $\eta V_{DD}$  in the output voltage and  $h = (V_{DD} - V_{min}) / (n - 1)$  is the step size. With parameter variations,  $V_{min}$  changes to  $V'_{min}$  and the new step size becomes  $h'$ . If we express  $h'$  in term of  $h$  as  $h' = \beta_1 h$  and  $\Delta'$  in term of  $\Delta$  as  $\Delta' = \beta_2 \Delta$ , then we can derive

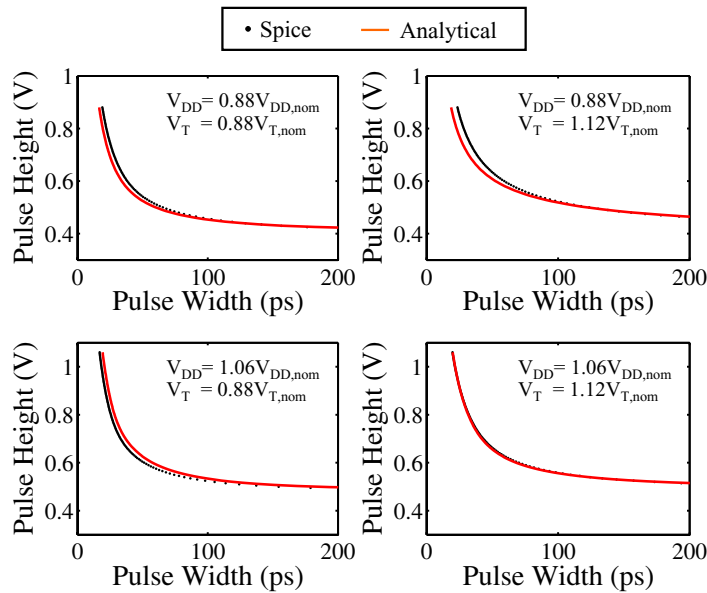


Figure 7: Comparison of the predicted and simulated NRCs for different combinations of  $V_{DD}$  and  $V_T$ .

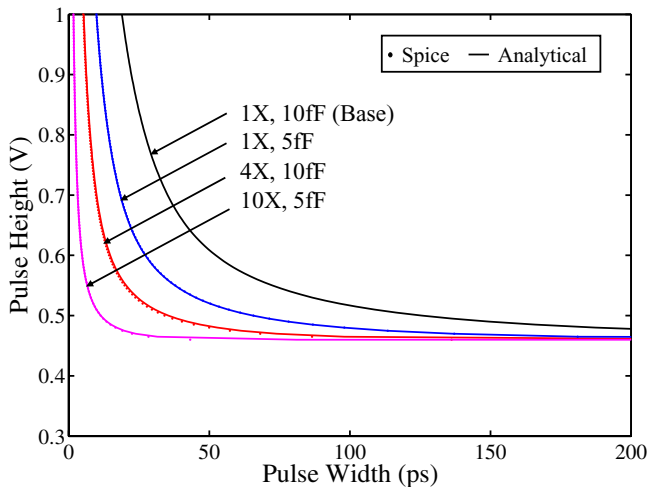


Figure 8: Comparison of the predicted and simulated NRCs for different gate sizes.

the new value of  $\psi$  from the base case susceptibility  $\psi_{\text{base}}$  using the trapezoidal rule of integration. Each trapezoid used for computing the area above the NRC gets scaled in height by  $\beta_1$  and width by  $\beta_2$ . Denoting  $\beta = \beta_1\beta_2$ , one can express the noise susceptibility for any case as

$$\psi = \beta\psi_{\text{base}} + (1 - \beta)(V_{DD} - V_{\text{min}})\Delta_{\text{max}} \quad (11)$$

where  $\Delta_{\text{max}}$  is the maximum pulse width under consideration, as defined in Section 2. The approximation used in this derivation is that the NRC is very close to  $V_{\text{min}}$  for a critical pulse width of  $\Delta_{\text{max}}$ . For all the cases displayed in Figures 5, 7 and 8, for  $n = 100$ , the average error in the estimation of the metric was found to be 0.5% whereas the maximum error was less than 2.5%.

## 5. Conclusions and future work

This paper showed that variability significantly impacts the noise robustness and reliability of logic gates. Analytical methods for efficient estimation of a noise susceptibility metric based on NRCs — in the presence of variability in  $L_{\text{eff}}$ ,  $V_T$ ,  $W$ , and  $V_{DD}$  — were described. Simulation results show that in comparison to SPICE simulations, the proposed method can accurately predict noise susceptibility for different values of these parameters. Directions for future research include (i) the development of algorithms that integrate the proposed models for noise susceptibility as design constraints into traditional power-delay optimization flows and (ii) the development of alternate metrics for noise susceptibility

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