

Simulation of transients caused by single-event upsets in combinational logic

Kartik Mohanram

Department of Electrical and Computer Engineering
Rice University, Houston, TX 77005
kmram@rice.edu

Abstract—A comprehensive technique for simulation of transients caused by single-event upsets (SEUs) in combinational logic circuits is described. Based upon linear RC models of gates, the proposed technique integrates a closed-form model for computation of the SEU-induced transient at the site of a particle strike with propagation models for the transients along a functionally sensitized path. A full set of simulation results indicate that on average, the models are accurate to within 10% of the results obtained using SPICE simulations (peak magnitude and duration about $0.5V_{DD}$) with over 1000X improvement in computational speed.

I. INTRODUCTION

Increasing design complexity and technology trends, including smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth are projected to cause an increase in the soft error failure rate in core combinational logic in sub-100 nm integrated circuits [1]–[5]. Soft errors occur as a result of single-event upsets (SEUs) caused by high-energy neutron and alpha particle strikes in integrated circuits. Although soft errors cause no permanent damage, they can severely limit the reliability of electronic systems.

As soft errors emerge as a reliability threat in mainstream commodity electronics [5], there is significant interest in the development of simulation techniques for SEUs and soft error failure rate analysis in integrated circuits. Introducing soft error analysis into the front-end of the design flow, at higher levels of design abstraction, provides the first means to assess the vulnerability of combinational logic circuits to SEUs. Based upon this analysis, robustness metrics can be used to identify and radiation harden logic blocks through reliability-aware logic synthesis and tuning of cell libraries. In addition, addressing soft error concerns at an early stage in the design cycle will facilitate convergence to inherently reliable solutions that meet area-delay-power objectives. This has cost and time-to-market benefits, since it will minimize iterations and time consuming rework during physical synthesis.

Central to all soft error analysis techniques in combinational logic is the simulation of SEU-induced transients at logic gates over a range of SEU particle energies (deposited charges) and their subsequent propagation through functionally sensitized paths. This is necessary in order to estimate the effects of masking factors – logical, electrical, and temporal – on the SEU as it propagates through the combinational logic circuit. Whereas several approaches for SEU modeling and simulation have been proposed in literature and are discussed in Sec. II,

there is no solution that is accurate, efficient, and directly compatible with present-day design flows.

This paper presents a comprehensive technique for simulation of transients caused by SEUs in combinational logic circuits. Based upon linear RC models of gates, the proposed technique integrates a closed-form model for computation of the SEU-induced transient at the site of a particle strike with propagation models for the transients along a functionally sensitized path. The proposed linear RC modeling technique resembles logical effort [6], [7] that is widely used to estimate gate and path delays in integrated circuits. The models are derived using a SPICE-based calibration of logic gates for a range of values of fanout, charge, and propagation path topologies. Closed-form solutions for SEUs along a propagation path in combinational logic circuits can be computed using the models. In addition to integration into tools for soft error failure rate analysis, the compatibility with load and performance constraints facilitate integration of these models with design automation tools for area-delay-power-reliability optimization. Cell library synthesis and characterization tools can also use these models to assess and design SEU-tolerant versions of cells subject to area-delay-power constraints. A full set of simulation results indicate that on average, the models are accurate to within 10% of the results obtained using SPICE simulations (peak magnitude and duration about $0.5V_{DD}$) with over 1000X improvement in computational speed.

The rest of this paper is organized as follows. In Sec. II, we provide some background and motivate the problem addressed here in greater detail. In Sec. III, we describe the linear model used to obtain closed-form expressions for the SEU-induced transients at the site of the particle strike. In Sec. IV, we describe linear RC models to compute the waveform for the transient as it propagates through gates on a functionally sensitized path. In Sec. V, we present the algorithm to calibrate gates for the proposed model. In Sec. VI, we present the simulation results. Section VII is a conclusion.

II. BACKGROUND AND MOTIVATION

There are two steps to simulation of SEUs in combinational logic circuits. The first step is the computation of the SEU-induced transient at the site of the particle strike. The next step involves the propagation of these SEU-induced transients along functionally sensitized paths to the primary outputs/latches/flip-flops. The identification of functionally

sensitized paths is usually performed using fault simulation. However, determination of the final magnitude and duration of the propagated pulse along a functionally sensitized path is computationally expensive, since it depends on the electrical properties of the intermediate gates along the path. SPICE or an equivalent circuit simulator can be used to account for electrical and temporal masking effects as a SEU originating at a sensitized node propagates to the primary outputs/latches/flip-flops. Since SEU simulation has to be performed for particle strikes over a range of deposited charge for each sensitized node for each input pattern, and since this analysis has to be repeated over tens of thousands of input patterns, even simple Monte Carlo and SPICE-based simulation techniques blow up very quickly on circuits with 100-200 gates.

Classical techniques for the analysis and simulation of SEU effects in combinational circuits fall into the device-, circuit-, and logic-level categories depending on their accuracy and computational complexity. Device-level approaches, such as [8]–[15], take into account interactions at the nuclear level, and yield accurate results at exorbitant computational cost. Whereas these can be used to guide post-layout analysis techniques, they do not scale well and cannot be used in the early phases of design space exploration. Logic-level approaches are abstraction-based, approximating SEU-induced transients by square or trapezoidal pulses with equivalent magnitude-duration profiles [16]–[18], and are mainly used for fault injection and simulation. Although these approaches scale well, they are inadequate from an accuracy standpoint for SEU simulation. This is because they lack the ability to cover a range of particle energies and SEU-induced transient profiles, and since they cannot account for non-linear pulse attenuation and amplification effects during propagation.

Circuit-level approaches constitute the middle ground between device-level and logic-level simulation approaches. Empirically verified circuit-level models, such as [19], use scaling factors to extend the base model for a 600 nm process technology to other feature sizes. SPICE-based circuit-level approaches, such as [20], depend on lookup tables and databases for SEU-induced transient simulation and propagation.

A second class of SPICE-based circuit-level approaches *separate* the computation of the SEU-induced transient from the propagation of this transient. Computation of the SEU-induced transient involves solving the transistor-level differential equation – explicitly, or implicitly through first-order models – to obtain a closed-form solution for the SEU-induced transient at the output of a logic gate. This is a non-linear second-order Riccati differential equation. The absence of a particular solution for the initial conditions precludes the existence of a general closed-form solution. Solutions proposed in literature include numerical analysis [21]–[23] and first-order RC modeling [24] for waveform and magnitude-duration analysis. For propagation of these SEU-induced transients, such circuit-level simulators use a set of propagation rules [24] and equivalent inverter models [18], [25] for gates.

In summary, previous methods proposed in literature suffer from one or more of the following disadvantages. They rely

on (i) equivalent inverter models for gates and (ii) square or trapezoidal approximations for SEUs. They also cannot (iii) accurately model varying fanout and combinations of gates along a propagation path, (iv) handle swings above V_{DD} and below ground, (v) account for non-linear amplification and attenuation effects on SEU-induced transients, and (vi) account for a range of charge deposited by particles of different energies. In this paper, we integrate the linear modeling technique proposed in [26] for SEU-induced transients at the site of a particle strike with linear RC-based propagation models to simulate SEUs over a range of particle charges in combinational logic circuits. The proposed technique is compatible with a combination of gates and load conditions along a functionally sensitized path, does not suffer from the shortcomings listed above, and is highly accurate in comparison to SPICE-based circuit-level simulation.

A. Simulation challenges

Consider a chain of 2-input NAND gates to several levels of logic as shown in Fig. 1. At each level of logic, a NAND gate drives two identical gates, to two levels of logic to approximate loading conditions (described in Sec. V). In other words, this is a fanout-of-2 (FO2) chain of 2-input NAND gates along which we study the propagation of a SEU-induced transient. In Fig. 1, the site of the particle strike is denoted by node n and is the output of the first NAND gate in the chain. The charge deposition due to a particle strike at the output n of the NAND gate is modeled by a double exponential current pulse $I_{in}(t)$ at n [27], [28]:

$$I_{in}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta} \right) \quad (1)$$

where Q is the charge (positive or negative) deposited as a result of the particle strike, τ_α is the collection time-constant of the junction, and τ_β is the ion-track establishment time-constant. τ_α and τ_β are constants that depend on several process-related factors. Note that $\lim_{t \rightarrow \infty} \int_0^t I_{in}(t) dt$ equals Q for conservation of charge.

A transient to logic 1 (logic 0) refers to the case when the steady-state logic value at n is logic 0 (logic 1) in the fault-free case and a SEU generates a positive (negative) transition to logic 1 (logic 0) at n . Without loss of generality, this discussion focuses on the simulation of $0 \rightarrow 1$ SEU-induced transients. Both inputs of the NAND gate are set to logic 1, so that the voltage is 0 at n in the fault-free case. The worst-case transient occurs when the site for the particle strike is the gate output, since transients at internal nodes are reduced in severity before they propagate to the output of the gate. The output responses of the NAND gates in the FO2 chain determined using SPICE simulations to a SEU that produces a $0 \rightarrow 1$ transient at n is shown in Fig. 1. The output nodes are denoted by V_1 , V_2 , and V_3 in the figure.

Two different charges were used for the simulations. When the deposited charge is 0.18 pC, it is clear from the figure that the peak value of the SEU-induced transient exceeds V_{DD} for the process (1.2 V). However, the propagated transients at V_1 ,

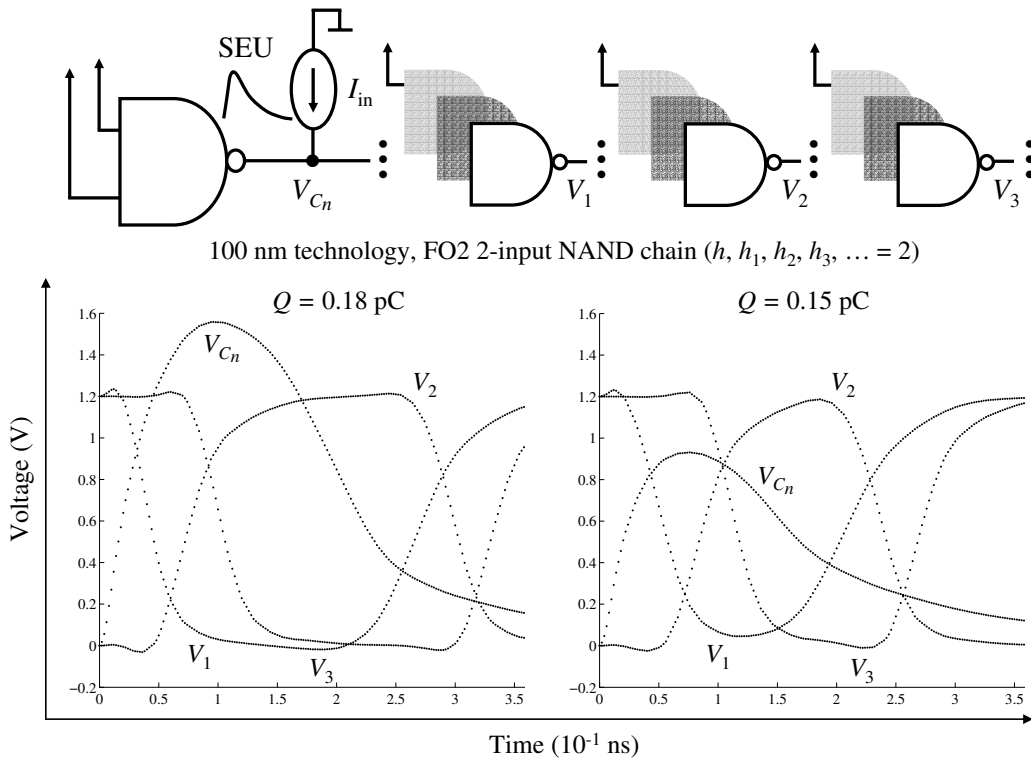


Fig. 1. Waveforms for FO2 2-input NAND chain (100 nm technology) obtained from SPICE simulations

V_2 , etc. may have no more than a full voltage swing along the sensitized path. The ability of strikes to cause V_{C_n} to exceed (drop below) V_{DD} (ground) also requires that a distinction be made between gates immediately in the fanout of the site of the particle strike and those that are several levels of logic removed from the site of the strike. When the charge deposited is 0.15 pC, the SEU-induced transient at n has a peak magnitude that is less than V_{DD} for the process. But the non-linear nature of the NAND gates result in an amplification of this transient such that it has a full voltage swing as it propagates along the fanout. The models proposed in this paper account for these effects and can be used to obtain closed-form expressions for the waveform of the SEU-induced transient as it propagates through the logic circuit.

III. SEU-INDUCED TRANSIENTS

In this section, we briefly review the linear model proposed in [26] for the computation of the waveform of the SEU-induced transient at the site of the particle strike. The model can be used to obtain both magnitude and duration of the transient waveform at the site of the strike. Further, the model integrates gate scale factor ξ and load (through fanout h) that are central to post-mapping transformations such as gate resizing, fanout optimization, resynthesis and remapping, etc. [29] making it compatible with synthesis tools for SEU-robustness evaluation and design.

The differential equation for the SEU-induced transient at

the output of the particle strike n in Fig. 1 is given by:

$$C_n \frac{dV_{C_n}}{dt} = I_{in}(t) - I_D(t) \quad (2)$$

where C_n is the total load capacitance (load and parasitic) at n , $I_{in}(t)$ is the double exponential current pulse modeling the SEU, and $I_D(t)$ is the current through the nMOS transistor network restoring the output to its fault-free value. Note that C_n equals $\xi(C_o + hC_l)$, since ξ scales both the gate and its fanout. Since $I_D(t)$ is non-linear in V_{C_n} , the differential equation is equivalent to a non-linear second-order Riccati differential equation with no closed-form solution. Instead, we turn to the method of logical effort [6], [7] that has been widely used in a variety of application domains as well as in industry standard tools for electronic design automation. Logical effort is based on a reformulation of the conventional RC model of CMOS gate delay which separates the effects of gate size, topology, parasitics, and load. Using logical effort, the delay τ of a gate with input capacitance C_i is estimated by modeling it as a linear function of the load C_l being driven and is given by $gh + p$ where g is the logical effort, h equals C_l/C_i is the electrical effort (and hence fanout), and the parasitic delay p is the intrinsic delay of the gate.

A. Three-parameter linear model $\tau_n(h, Q, \xi)$

Consider Fig. 2 that presents a linear RC model for the NAND gate from Fig. 1 that is analogous to the model used for logical effort. R_D is the equivalent resistance that models the effects of the nMOS transistors that dissipate the charge and

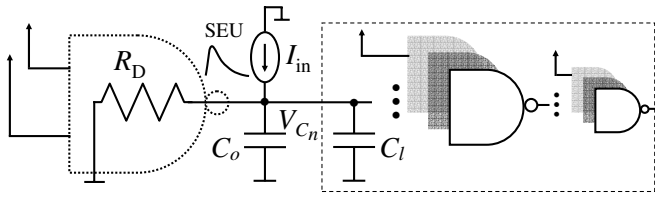


Fig. 2. Linear RC model for NAND gate when a particle strike occurs at its primary output. The nMOS transistor network is replaced by the equivalent resistance R_D .

restore n to its original value. The product $R_D C_n$ is denoted by τ_n – it can be interpreted as a *recovery time constant* that reflects the ability of the transistors to dissipate the deposited charge to restore the node to its original logic value. A linear model for τ_n , along the lines for delay τ in logical effort, as a function of the particle charge Q , the fanout h , and the gate scale factor ξ is given by:

$$\tau_n = a_0 + a_h h + a_Q Q + a_\xi \xi \quad (3)$$

where a_0 , a_h , a_Q , and a_ξ are constants determined using the calibration techniques from [26] and summarized in Sec. V.

With this model, the differential equation for the SEU-induced transient at the output of the NAND gate in Fig. 2 is given by:

$$C_n \frac{dV_{C_n}}{dt} = I_{in}(t) - \frac{V_{C_n}}{R_D} = I_{in}(t) - \frac{C_n V_{C_n}}{\tau_n} \quad (4)$$

This is a first-order differential equation whose solution can be obtained through the use of integrating factors. The final solution to the transient waveform $V_{C_n}(t)$, when $\tau_n < \tau_\alpha$ that is the the most commonly encountered case for logic gates for nominal values of τ_α , is given by

$$V_{C_n}(t) = \frac{Q}{C_n} \frac{\tau_n}{(\tau_\alpha - \tau_n)} \left(e^{-t/\tau_\alpha} - e^{-t/\tau_n} \right)$$

Without loss of generality, the parameter τ_β that controls the rise time of $I_{in}(t)$ is ignored for the rest of this discussion. Note that all the analysis is easily extended to (i) double exponential models for the injected current with non-zero τ_β and (ii) $1 \rightarrow 0$ SEU-induced transients – both are described in detail in [26].

Fig. 3 presents the results for the 2-input NAND gate in 100 nm technology when τ_n is modeled as a function of fanout h , charge Q , and scale factor ξ . The solution for τ_n was obtained following the calibration runs described in Sec. V. The graphs shown in the curve are for three arbitrary pairs chosen in the the calibrated space. Since SEU simulation is always run on a fixed library of gates, ξ is always fixed for all the gates in the library. We thus focus on a two-parameter model $\tau_n(h, Q)$ for the rest of this paper.

IV. PROPAGATION OF SEU-INDUCED TRANSIENTS

The necessity to reproduce the waveforms of the SEU-induced transients along a functionally sensitized propagation path arises since soft error analysis depends on accurate simulation of electrical and temporal effects on such transients.

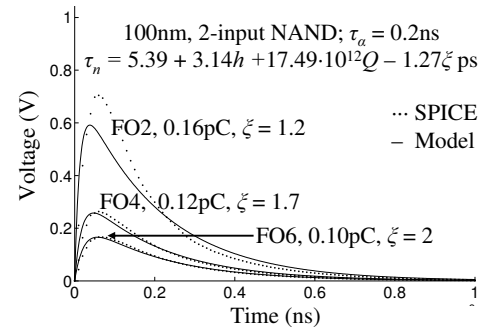


Fig. 3. Transient waveforms for 2-input NAND gate in 100 nm technology. τ_n was calibrated as a function of fanout h , charge Q , and scale factor ξ [26].

Let i denote the distance of the gate on the sensitized path from the site of the strike. For each logic gate (other than the site of the particle strike) on the sensitized path for SEU-induced transient propagation, there are three parameters that are required to reconstruct the waveform. These are the propagation time-constants for rising and falling edges of the transients denoted by τ_{pr}^i and τ_{pf}^i , the minimum and maximum values of voltage of these transients denoted by V_{min}^i and V_{max}^i , and the time instants at which the rise and fall of the propagated transients begin and end at the gate denoted by t_{pf}^i and t_{pr}^i . In the next three sub-sections, we describe how these quantities are defined and measured from the SPICE simulations of the calibration structure described in Sec. V.

The models for propagation of SEU-induced transients are classified based on the distance (i.e., levels of logic) that separate the gate from the site of the particle strike. Gates with index i equals 1, i.e., gates in the immediate fanout of the site of the strike, are analyzed separately from gates that are at a distance of two or more levels of logic from the site of the strike for two reasons. First, the waveform at the input of a gate with index 1 has the capability to rise above V_{DD} (or fall below 0) for large charges. Second, the double-exponential nature of the voltage $V_{C_n}(t)$ driving the gate has a form and slew rate altogether different from single-pole exponential waveforms of the type encountered at the outputs of logic gates.

A. Propagation time-constants τ_{pr}^i and τ_{pf}^i

Without loss of generality, consider the NAND gate at distance 1 from the site of the particle strike. A $0 \rightarrow 1$ transient at n produces a $1 \rightarrow 0$ transient at the output of this gate. Since the fanout gates reproduce waveforms delayed by an amount equal to the propagation delay of the gate, the shape of the propagated waveform is very similar to the stimulus. In logical effort, the $gh + p$ form for the propagation time-constant τ reflects the fact that the only factor that influences the propagation delay is the fanout of the gate. Analogous to logical effort, a first-order RC model for the propagation time-constant for the falling transition at V_1 is denoted by τ_{pf}^1 . However, for SEUs, the shape of the stimulus varies depending upon the deposited charge Q and the fanout h at the site of the strike. Thus, in the absence of a universal stimulus waveform (assumed for logical effort), the linear model for the

propagation time-constants must include the effects of both h and Q . Since the shape of the SEU-induced waveform is determined by the recovery time constant τ_n of the gate at the site of the strike, and since it accounts for both h and Q at the site of the strike, the propagation time-constants τ_{pf}^1 and τ_{pr}^1 are modeled as functions of local fanout h_1 and the shape of the input stimulus τ_n .

For gates at a distance 2 and higher, the propagation time-constants are modeled as a function of the shape of the stimulus in addition to the local fanout h_i . Since the shape of the rising and falling edges at i is influenced by τ_{pf}^{i-1} and τ_{pr}^{i-1} of the $(i-1)^{\text{th}}$ gate respectively, linear approximations for the propagation time-constants are given by the following expressions:

$$\tau_{pf}^i = \begin{cases} \tau_{pf}^1(\tau_n, h_1) & : i = 1 \\ \tau_{pf}^i(\tau_{pr}^{i-1}, h_i) & : i \geq 2 \end{cases}$$

$$\tau_{pr}^i = \begin{cases} \tau_{pr}^1(\tau_n, h_1) & : i = 1 \\ \tau_{pr}^i(\tau_{pf}^{i-1}, h_i) & : i \geq 2 \end{cases}$$

τ_{pf}^i and τ_{pr}^i are directly obtained from the calibration runs by measuring the time that the output waveform at V_i takes to rise (fall) from 0 (V_{DD}) to $0.5V_{DD}$.

B. Minimum and maximum voltages V_{\min}^i and V_{\max}^i

In addition to the propagation time-constants, the minimum and maximum voltages reached by these propagated transients is essential to reproduce the waveforms completely. As was shown in Fig. 1, the transients can have a swing that is less than the full range $\{0, V_{DD}\}$. Analogous to the propagation time constants, the minimum and maximum values of the transient voltage at each stage can be parameterized as functions of the shape of stimulus and the local fanout h_i . Linear approximations for the minimum and maximum values of the SEU-induced transients along a propagation path are given by the following expressions:

$$V_{\min}^i = \begin{cases} V_{\min}^1(\tau_n, h_1) & : i = 1 \\ V_{\min}^i(\tau_{pr}^{i-1}, h_i) & : i \geq 2 \end{cases}$$

$$V_{\max}^i = \begin{cases} V_{\max}^1(\tau_n, h_1) & : i = 1 \\ V_{\max}^i(\tau_{pf}^{i-1}, h_i) & : i \geq 2 \end{cases}$$

Note again that a distinction is made between gates at logic level 1 and gates that are two or more logic levels removed from the site of the particle strike.

C. Time instants t_{pf}^i and t_{pr}^i

With propagation time-constants and min-max values on the transients, the waveforms can be reproduced accurately at each of the nodes. However, it is necessary to include temporal information with the waveforms to obtain the exact time instants when the transient reaches nodes along the path. This

temporal information used to time-shift the waveforms can be calculated in a straightforward manner when we recognize that the propagation time-constants essentially correspond to the 50% crossing point (with a $\ln 2$ factor) on the input waveforms. In other words, a fanout gate turns on and begins a rising/falling transition when its input reaches $0.5V_{DD}$ in the falling/rising directions. Let t_{pf}^{i-1} (t_{pr}^{i-1}) be the time instant at which the input to a gate begins a falling (rising) transition. The time instance at which the output of the gate begins its rising (falling) transition is given by adding $\tau_{pf}^{i-1} \ln 2$ ($\tau_{pr}^{i-1} \ln 2$) to these time instants.

As explained before, gates at level 1 constitute a corner case, since the stimulus can have a peak larger (or smaller) than V_{DD} on a $0 \rightarrow 1$ ($1 \rightarrow 0$) transient. This is handled in a straightforward manner by modeling t_{pf}^1 and t_{pr}^1 as functions of the shape of the double-exponential stimulus, i.e., as functions of h and Q (and hence implicitly τ_n). Linear approximations for the time instants t_{pf}^i and t_{pr}^i used to reconstruct temporal information for the propagated waveforms are given by the following expressions:

$$t_{pr}^i = \begin{cases} t_{pr}^1(h, Q) & : i = 1 \\ t_{pf}^{i-1} + \tau_{pf}^{i-1} \ln 2 & : i \geq 2 \end{cases}$$

$$t_{pf}^i = \begin{cases} t_{pr}^1(h, Q) & : i = 1 \\ t_{pr}^{i-1} + \tau_{pr}^{i-1} \ln 2 & : i \geq 2 \end{cases}$$

D. Waveforms

The piece-wise expressions used to construct the waveforms for V_{C_n} , V_1 , V_2 , and V_3 are presented in Fig. 4. The waveforms are obtained by a straightforward traversal of all the gates along a functionally sensitized path. Since the waveforms corresponding to different charges can all be computed in a single pass (as opposed to multiple SPICE runs), significant computational savings are obtained since soft error analysis techniques simulate over a range of deposited charge (this corresponds to a range of incident particle energies). In Sec. VI, we present simulation results for several randomly generated combinational netlists to illustrate the computational accuracy and efficiency of the proposed method.

V. CALIBRATING THE MODEL

A single 3-stage calibration structure, based on the 4-stage structure proposed in [7] for logical effort analysis, is shown in Fig. 5. This structure can be used to calibrate the gates for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transients by setting the inputs to the gates appropriately. Note that the structure can also be used to calibrate gates for strikes at internal nodes in order to increase simulation accuracy. For a $0 \rightarrow 1$ SEU-induced transient, three sets of coefficients for each logic gate in the library for each combination of parameters h , Q , h_1 , and h_2 are given by

- 1) τ_n , when the gate is the site of the particle strike,
- 2) τ_{pf}^1 and τ_{pr}^1 , V_{\min}^1 , and t_{pf}^1 and t_{pr}^1 when the gate is driven by a gate at whose output the particle strike occurs, and

$$\begin{aligned}
V_{C_n}(t) &= \frac{Q}{C_n} \frac{\tau_n}{(\tau_\alpha - \tau_n)} \left(e^{-t/\tau_\alpha} - e^{-t/\tau_n} \right) & : 0 \leq t \leq t_{\max} \\
V_1(t) &= \begin{cases} V_{DD} & : 0 \leq t \leq t_{pf}^1 \\ V_{DD} - (V_{DD} - V_{\min}^1) \left(1 - e^{-(t-t_{pf}^1)/\tau_{pf}^1} \right) & : t_{pf}^1 < t \leq t_{pr}^1 \\ V_{DD} - (V_{DD} - V_{\min}^1) \left(e^{-(t-t_{pr}^1)/\tau_{pr}^1} \right) & : t_{pr}^1 \leq t < t_{\max} \end{cases} \\
V_2(t) &= \begin{cases} 0 & : 0 \leq t \leq t_{pr}^2 \\ V_{\max}^2 \left(1 - e^{-(t-t_{pr}^2)/\tau_{pr}^2} \right) & : t_{pr}^2 \leq t < t_{pf}^2 \\ V_{\max}^2 \left(e^{-(t-t_{pf}^2)/\tau_{pf}^2} \right) & : t_{pf}^2 < t \leq t_{\max} \end{cases} \\
V_3(t) &= \begin{cases} V_{DD} & : 0 \leq t \leq t_{pf}^3 \\ V_{DD} - (V_{DD} - V_{\min}^3) \left(1 - e^{-(t-t_{pf}^3)/\tau_{pf}^3} \right) & : t_{pf}^3 < t \leq t_{pr}^3 \\ V_{DD} - (V_{DD} - V_{\min}^3) \left(e^{-(t-t_{pr}^3)/\tau_{pr}^3} \right) & : t_{pr}^3 \leq t < t_{\max} \end{cases}
\end{aligned}$$

Fig. 4. Expressions used to construct the waveforms along the SEU's propagation path

- 3) τ_{pf}^i and τ_{pr}^i , and V_{\max}^i when the gate is $i \geq 2$ levels of logic from the site of the strike. V_{\min}^i for $i \geq 2$ is approximated using the expression $(V_{DD} - V_{\max}^{(i-1)})$.

In logical effort, two preliminary stages are used to shape the slope of the stimulus. Here, this is replaced by the first stage that contains the gate under calibration. A current source at the output (and not the input) of the gate under calibration serves as the stimulus. With respect to the first stage, the second and third stages are there to serve as a load on the first stage. Each stage contains a primary gate (a), a load gate (b), and a load on the load (c). Gate (c) is essential to model the gate-drain overlap capacitance and prevents the output of gate (b) from switching rapidly. Gate (a) in the first stage is the gate under calibration; its inputs have stabilized and its output is the site of a particle strike. All side inputs are set to non-controlling values to allow the propagation of the SEU-induced transient through the stages.

Similarly, the second and third stages are present to calibrate the gate's propagation properties to SEU-induced transients at its inputs. When the gates (b) and (c) that load the third stage are accounted for, the 3-stage structure has a total depth of five logic levels. In [26], h_1 and h_2 were equal to h in the second and third stages. However, to factor varying fanout conditions along a propagation path, h_1 and h_2 are allowed to vary independently over the range $\{1, h_{\max}\}$ increasing the number of calibration runs that need to be performed.

The pseudo-code for the procedure used to calibrate the gate in the test structure for a range of values of h , Q , h_1 , and h_2 is given in Fig. 6. Besides the range of values for fanout h , h_1 , and h_2 , the range of values for charge Q is determined by process-related factors (see Sec. V-A). Each SPICE run is used to measure and populate the entries of all the \mathcal{M} matrices shown in Fig. 6 except \mathcal{M}_{τ_n} . In order to populate \mathcal{M}_{τ_n} , τ_n is obtained from the simulation trace using the technique described in [26] as follows. Using the average

values of voltage V_{C_n} and current I_{C_n} over the simulation interval $[0, \tau_\alpha]$, τ_n can be obtained by rearranging the terms in the integrated form of Eqn. 4 to obtain:

$$\tau_n = \frac{C_n \int_0^{\tau_\alpha} V_{C_n}(t) dt}{Q (1 - e^{-\tau_\alpha/\tau_n}) - \int_0^{\tau_\alpha} I_{C_n}(t) dt} \quad (5)$$

There is an entry corresponding to each combination of free variables h , Q , h_1 , and h_2 in the matrices. Robust linear regression based on an iteratively re-weighted least squares algorithm (function `robustfit` in MATLAB) is then run on each of the \mathcal{M} matrices to obtain the coefficients for the linear models.

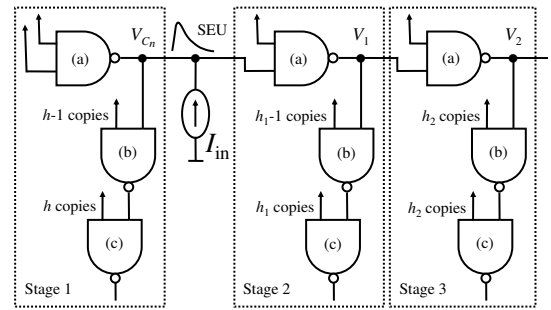


Fig. 5. Proposed test structure to calibrate the model.

A. Choosing charge

Upper bounds on the charge used for calibration are determined as follows. The term linear energy transfer (LET) is used to describe the sensitivity of a process technology to SEUs. A particle with a LET of $1 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ deposits approximately $10 \text{ fC}/\mu\text{m}$ of electron-hole pairs along its track [3], [30]. The LET of very few ionizing particles in silicon is higher than $15 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ [31], [32]. The LET of a particle is multiplied by the charge collection depth to obtain the total electron-hole pairs generated by a strike. For process

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 $h_{\max}$  – maximum allowed fanout ( $h, h_1, h_2$ ) for gate-under-calibration
 $Q_{\max}$  – maximum calibration charge for process technology
 $\tau_{\alpha}$  – junction collection time-constant for the process technology
 $\mathcal{M}_{\tau_n}$  – Matrix with calibration entries for  $\tau_n$ 
 $\mathcal{M}_{\tau_{pf}^1}, \mathcal{M}_{\tau_{pr}^1}, \mathcal{M}_{V_{\min}^1}, \mathcal{M}_{t_{pf}^1}$ , and  $\mathcal{M}_{t_{pr}^1}$  – Calibration matrices for level  $i = 1$  gates
 $\mathcal{M}_{\tau_{pf}^i}, \mathcal{M}_{\tau_{pr}^i}$ , and  $\mathcal{M}_{V_{\max}^i}$  – Calibration matrices for level  $i \geq 2$  gates
for  $h \leftarrow 1$  to  $h_{\max}$  by 1
  for  $Q \leftarrow Q_{\max}/5$  to  $Q_{\max}$  by  $Q_{\max}/5$ 
    for  $h_1 \leftarrow 1$  to  $h_{\max}$  by 1
      for  $h_2 \leftarrow 1$  to  $h_{\max}$  by 1
        do RUN-SPICE( $h, Q, h_1, h_2, \tau_{\alpha}$ )
           $\tau_n \leftarrow$  COMPUTE- $\tau_n(h, Q, \tau_{\alpha})$ ; UPDATE( $\mathcal{M}_{\tau_n}, \tau_n, h, Q,$ )
          MEASURE-AND-UPDATE( $\mathcal{M}_{\tau_{pf}^1}, \tau_n, h_1$ ); MEASURE-AND-UPDATE( $\mathcal{M}_{\tau_{pr}^1}, \tau_n, h_1$ )
          MEASURE-AND-UPDATE( $\mathcal{M}_{V_{\min}^1}, \tau_n, h_1$ )
          MEASURE-AND-UPDATE( $\mathcal{M}_{t_{pf}^1}, h, Q$ ); MEASURE-AND-UPDATE( $\mathcal{M}_{t_{pr}^1}, h, Q$ )
          MEASURE-AND-UPDATE( $\mathcal{M}_{\tau_{pf}^1}, \tau_{pr}^1, h_2$ ); MEASURE-AND-UPDATE( $\mathcal{M}_{\tau_{pr}^1}, \tau_{pf}^1, h_2$ )
          MEASURE-AND-UPDATE( $\mathcal{M}_{V_{\max}^1}, \tau_{pf}^1, h_2$ )
         $\tau_n(h, Q) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{\tau_n}$ )
         $\tau_{pf}^1(\tau_n, h_1) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{\tau_{pf}^1}$ );  $\tau_{pr}^1(\tau_n, h_1) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{\tau_{pr}^1}$ )
         $V_{\min}^1(\tau_n, h_1) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{V_{\min}^1}$ )
         $t_{pf}^1(h, Q) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{t_{pf}^1}$ );  $t_{pr}^1(h, Q) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{t_{pr}^1}$ )
         $\tau_{pf}^i(\tau_{pr}^{i-1}, h_i) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{\tau_{pf}^i}$ );  $\tau_{pr}^i(\tau_{pf}^{i-1}, h_i) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{\tau_{pr}^i}$ )
         $V_{\max}^i(\tau_{pf}^{i-1}, h_i) \leftarrow$  RUN-LINEAR-REGRESSION( $\mathcal{M}_{V_{\max}^i}$ )

```

Fig. 6. CALIBRATE-GATE($h_{\max}, Q_{\max}, \tau_{\alpha}$) for $0 \rightarrow 1$ SEU-induced transients

technologies of 180 nm and higher, the charge collection depth does not change significantly and is typically 2 microns in epitaxial (as well as bulk) substrates [3], [33]. This gives an upper bound of 0.3 pC for 180 nm process technologies. For smaller feature sizes, the charge collection efficiency decreases primarily due to higher channel doping density and a decrease in active layer thickness, which reduces depletion width and channel funneling [27], [33], [34]. In [19], an inverse linear relation between collected charge and doping density was determined empirically. For example, since uniform technology scaling [35] increases doping density by a factor of λ (equals $\sqrt{2}$) in successive process technologies, upper bounds of 0.21 pC, 0.15 pC, and 0.11 pC can be derived for 130 nm, 100 nm, and 70 nm process technologies. In Sec. VI, we use the actual values of doping density to scale the base value of 0.30 pC to obtain the calibration limit for smaller process technologies.

VI. SIMULATION RESULTS

The SPICE libraries for four process technologies – 180 nm, 130 nm, 100 nm, and 70 nm – were obtained from the Berkeley predictive technology model [36]. We used $\tau_{\alpha} = 0.2$ ns and $\tau_{\beta} = 0$ in all our simulations. The maximum charges used for calibration of each process technology are presented in Table I. The charges were derived based on the discussion presented in Sec. V-A. The doping densities for the n-channel were obtained from the SPICE files and used to scale the base

charge of 0.30 pC for a 180 nm technology¹. Note that these values are only a guideline to determine the maximum charge for a process technology.

TABLE I
MAXIMUM CHARGE USED FOR CALIBRATION

Process technology (nm)	Doping density (cm ⁻³)	Charge (pC)
180	$5.9 \cdot 10^{17}$	0.30
130	$5.6 \cdot 10^{17}$	0.30 ¹
100	$9.7 \cdot 10^{17}$	0.18
70	$12.0 \cdot 10^{17}$	0.15

A. FO2 2-input NAND CHAIN

We first return to the example used in the motivation (Fig. 1) and compare the waveforms obtained using the proposed simulation technique (solid curves) with the reference waveforms obtained through SPICE simulations (dotted curves) in Fig. 7. It is clear from the figure that the results obtained using the proposed method are in excellent agreement with the results obtained using SPICE simulations, both in terms of magnitude and duration of the propagated transients.

B. Arbitrary propagation path

In order to verify that the technique works with arbitrary combinational logic networks, we implemented a random

¹The doping density for the 130 nm process technology does not follow the scaling trend. However, for consistency, we did not alter this and used 0.30 pC as the worst-case charge for the 130 nm process technology.

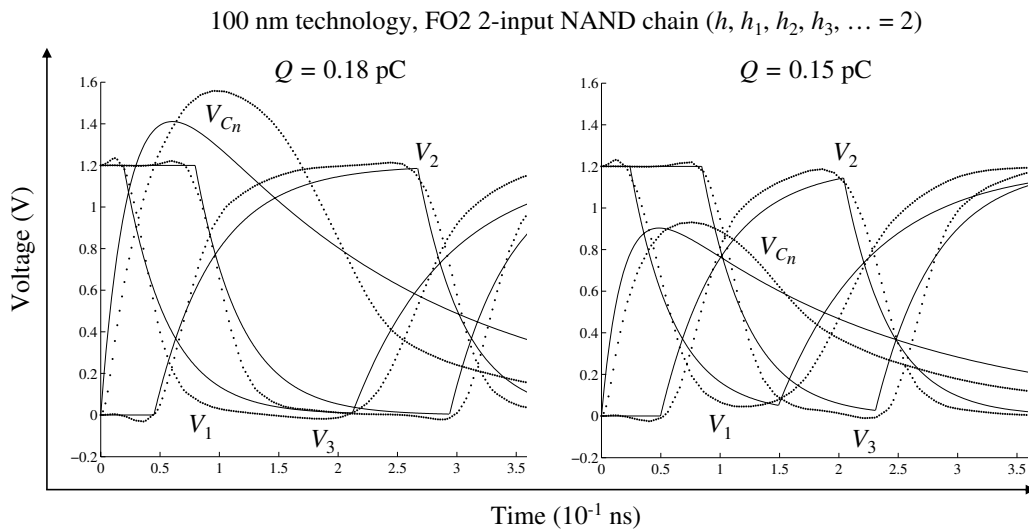


Fig. 7. Waveforms for FO2 2-input NAND chain (100 nm technology) obtained using proposed method (solid curves) and SPICE simulations (dotted curves).

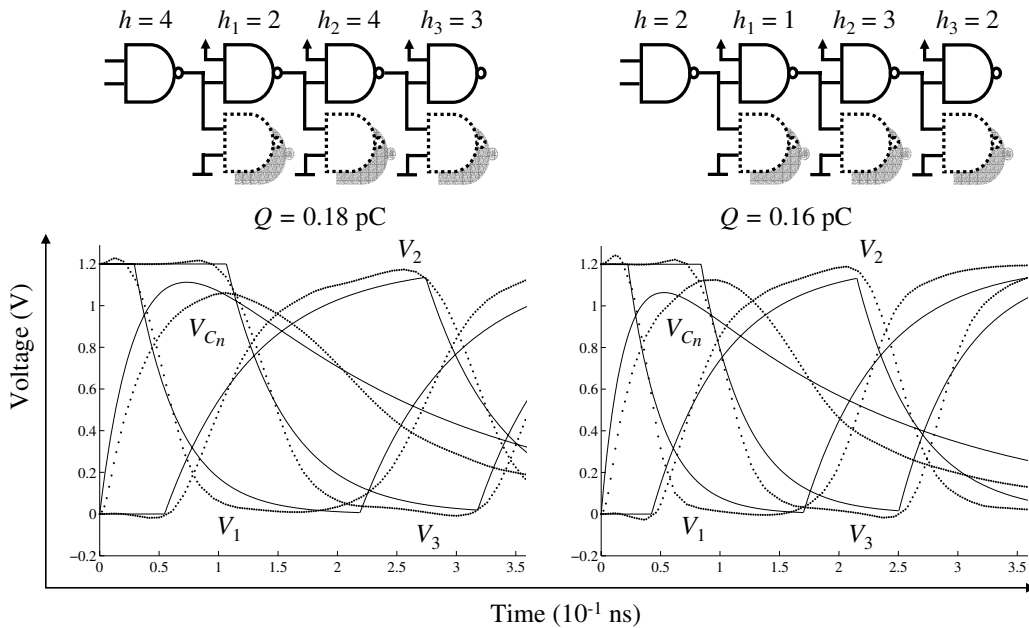


Fig. 8. Waveforms obtained for SEU propagation along arbitrary functionally sensitized propagation paths extracted from randomly generated netlists and random particle charge. The solid (dotted) curves are obtained using the proposed method (SPICE simulations).

netlist generator. The propagation paths were then extracted and all side inputs of other fanout gates on the path were set to controlling values. Thus, the SEUs could propagate along only one functionally sensitized path. The functionally sensitized path was then extracted and the SEU was simulated using SPICE as well as the proposed method to a logic depth of 4 gates. The waveforms for two out of several simulated cases are presented in Fig. 8. For the case with Q equals 0.18 pC (0.16 pC), the fanout along the propagation path was $\{4,2,4,3\}$ ($\{2,1,3,2\}$). As explained above, only one propagation path was chosen for simulation. When the case with the ability for a SEU to propagate along more than one fanout gate is encountered, the two different propagation paths can be

analyzed separately by assuming that only one path is active at any instant in time. This is a conservative approach and ensures that worst-case transients are propagated. The final magnitude and duration of the transient due to reconvergent fanout and propagation along multiple paths to the same output gate is handled by expanding overlapping arrivals and considering the maximum of the propagated transients. Our simulation results indicate that on average, the magnitude and duration about $0.5V_{DD}$ of the propagated transient obtained using the proposed model is accurate to within 10% of the results obtained using SPICE with over 1000X improvement in computational speed.

VII. CONCLUSION

In the future, as the soft error failure rate of logic circuits becomes unacceptably high even for mainstream applications, high-level SEU analysis and robustness techniques will play a critical role in accelerating convergence to SEU-tolerant designs. A comprehensive technique for simulation of transients caused by SEUs in combinational logic circuits was described in this paper. Based upon linear RC models of gates, the proposed technique is compatible with a range of charge deposition as well as propagation paths with varying fanout, topology, and types of gates. The close similarity to logical effort, high accuracy, and computational ease makes it attractive for integration into design automation tools.

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