A Model-Based Technique for Efficient Evaluation of Noise Robustness

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***Abstract*— In this paper, we present an analytical technique for deriving noise rejection curves (NRCs) and the associated noise susceptibility metric under parameter variations (L_{eff}, V_{T}, V_{DD} and channel width, W). The method involves modeling of the pull-up and pull-down resistances using approximated BSIM4 device equations. Compared to circuit simulation results, the analytical model provides more than five orders of magnitude speedup while maintaining an average (maximum) error of 1.3% (5%) over the entire range of parameter variations, which makes it suitable for design optimization for noise robustness.**

I. Introduction

The existence of considerable variability in deep submicron integrated circuits is a major concern for designers since the actual performance can vary drastically from the predicted performance leading to yield loss. The effect of process variations on timing and power has been the subject of extensive research in both academia and industry [1]–[7]. However, the impact of variability on the noise immunity, which decreases with aggressive technology scaling into the sub-100nm regime, remains largely unexplored.

Whether a noise pulse of any kind can cause instability in a gate depends on the susceptibility of the gate to input noise, which is an intrinsic property of the gate. With parameter variations The noise immunity of a gate can vary significantly. The use of static noise margin (SNM) as the metric for noise robustness can be overly pessimistic for transient pulses. A new metric based upon noise rejection curves (NRCs) was proposed in [8] to incorporate the pulse magnitude-duration information captured in the NRCs and thereby to remove the pessimism associated with SNM based metrics. The target of [8] was to (1) capture the effect of parameter variations on noise robustness and (2) circuit optimization with noise robustness as one objective. To facilitate quick estimation of the noise susceptibility metric, an analytical model for the noise susceptibility metric was also developed.

The model presented in [8] consists of a single equivalent resistance of the pull-up and the pull-down paths and thus cannot handle the independent variations of parameters in the pull-up and pull-down networks. However, the impact of parameter variations on noise is more prominent when the mismatch between the pull-up and pull-down networks is greater. In this paper, we extend our former model and complete the analytical modeling of NRCs. We present a BSIM4 equation-based resistance model for the pull-up and pull-down networks and thereby derive the noise rejection curves without performing expensive circuit simulations. The model can predict the effect of parameter variations (namely L_{eff}, V_{T}, W and V_{DD}) on the noise rejection curves accurately.

II. Noise Susceptibility and Parameter Variation

A noise pulse can be characterized by its magnitude (H) and duration (Δ). A gate is said to reach the point of instability under an applied noise pulse if H is greater than the SNM, and Δ exceeds a critical value, Δ_{c}. Instability is defined with respect to a preset voltage, ηV_{DD} ($0 < \eta < 1$), by which the output voltage of the affected gate must deviate from its steady-state value. Therefore, at time Δ_{c} the output voltage reaches the critical value V_{c}, which is $(V_{\mathrm{DD}} - \eta V_{\mathrm{DD}})$ for falling output transition and $\eta V_{\mathrm{DD}})$ for rising output transition to drive the gate to instability. Noise rejection curves (NRCs) factor in such magnitude versus critical duration profiles for noise pulses. In [8], we proposed a new metric — noise susceptibility (ψ) — that is given by the area above the NRC up to a maximum pulse duration, $\Delta_{\max}$ and thereby abstracts the information contained in an NRC to a single value.

Noise pulses with heights much smaller than the values predicted by NRCs can drive a gate to instability under parameter variations [8]. Determination of noise susceptibility under parameter variations, therefore, is crucial for robust circuit design. Monte Carlo based circuit simulations can reveal the dependence between noise susceptibility and parameter variations accurately, but at the cost of high computational expenses. This motivates the development of a generalized analytical technique for deriving NRCs and the associated ψ metric.

III. Analytical Models

We model a CMOS gate with three elements: a pull-up resistance (R_{pu}), a pull-down resistance (R_{pd}) and an output capacitance (C_{eq}), as shown in Figure 1. The value of each of these elements is function of the gate size, the device parameters, as well as the input and the output voltages. The main problem in analytically deriving the noise rejection curves is the nonlinearity associated with the devices present in the gates. Since the operating region of the different MOSFETs varies with the input pulse height and the rising/falling output node voltage, the effective resistances of the pull-up and pull-down paths are highly dependent on the operating point. However, under different simplified assumptions, we develop an efficient analytical model, which will be accurate enough for the purpose of design optimization.

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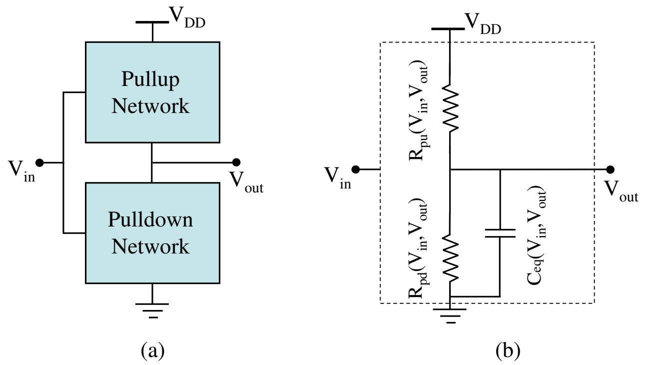

Figure 1. (a) General structure of a CMOS gate represented as a combination of a pull-up and a pull-down network. (b) Equivalent circuit representation of the gate where the cell is represented by three elements: a pull-up resistance, a pull-down resistance and an output capacitance.

For a rising pulse applied at the input of an inverter, the output is assumed to be initially charged to $V_{\rm DD}$. While discharging the output from $V_{\rm DD}$ to $V_{\rm c} = (1-\eta)V_{\rm DD}$, the NMOS transistor is operating in the saturation region. The pull-down equivalent resistance ($R_{\rm pd}$) is computed by the average of the resistance values at the two endpoints, $V_{\rm DD}$ and $(1-\eta)V_{\rm DD}$, as in [9]:

$$R_{\rm pd} = \frac{1}{2}\left[\frac{V_{\rm DD}}{I_{\rm Dsat}\left(1+\lambda_{\rm n}V_{\rm DD}\right)} + \frac{(1-\eta)V_{\rm DD}}{I_{\rm Dsat}\left(1+\lambda_{\rm n}(1-\eta)V_{\rm DD}\right)}\right] \quad (1)$$

$$\text{with } I_{\rm Dsat} = K_{\rm n}\frac{W}{L}\left[\left(H - V_{\rm T,n}\right)V_{\rm Dsat} - \frac{V_{\rm Dsat}^2}{2}\right],$$

where $\lambda_{\rm n}$ is the channel-length modulation parameter, $K_{\rm n}$ is the transconductance parameter, and $V_{\rm Dsat}$ is the saturation drain voltage.

For the same rising pulse, the PMOS transistor operation (where $|V_{\rm GS}| = V_{\rm DD} - H$) extends from the subthreshold to the linear region. The pull-up resistance of the PMOS transistor is negligible with respect to the pull-down transistor when the former works in the subthreshold region while the latter works in the saturation mode. We model the pull-up resistance only in the linear operation region of the PMOS transistor since the subthreshold operation contributes insignificantly to $R_{\rm eq}$:

$$R_{\rm pu} = \frac{\eta V_{\rm DD}}{K_{\rm p}\frac{W}{L}\left(V_{\rm DD} - H - V_{\rm T,p}\right)^2}\frac{1}{1+\lambda_{\rm p}V_{\rm DD}\left(1-\frac{\eta}{2}\right)}. \quad (2)$$

$V_{\rm T}$ is function of the effective gate length ($L_{\rm eff}$) and the drain-source voltage ($V_{\rm DS}$) due to the Drain Induced Barrier Lowering (DIBL) effect in short channel devices. In our case, the DIBL effect is very important since it causes considerable deviation between the analytical model and the SPICE simulation, especially when studying the ($L_{\rm eff}$) variability. To increase the accuracy of our analytical model, we have included the DIBL effect as shown in Equation 3, adopted from the BSIM4 MOSFET model [10].

$$V_{\rm T} = V_{\rm TH0} - \frac{\eta_0 V_{\rm DS}}{2\cosh\left(D_{\rm SUB}\frac{L_{\rm eff}}{L_{\rm t}}\right) - 1}. \quad (3)$$

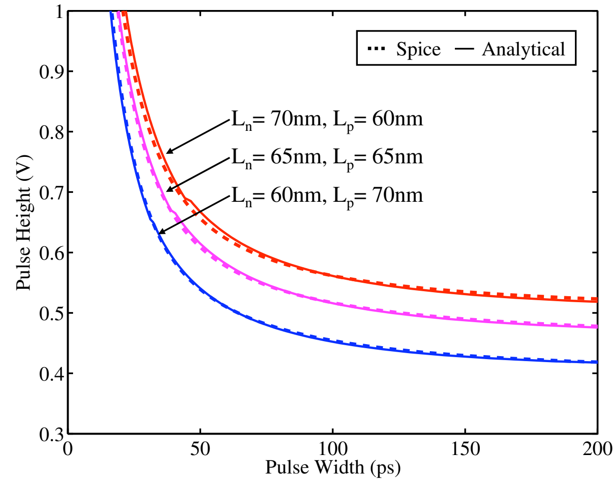

Figure 2. Comparison of the predicted and simulated NRCs for different combination of gate lengths.

Here the BSIM4 model parameters: $V_{\rm TH0}$ is the long-channel threshold voltage at zero body bias, η_0 is the DIBL coefficient in subthreshold region, $D_{\rm SUB}$ is the DIBL coefficient exponent in subthreshold region. The effective channel length $L_{\rm eff} = L + X_{\rm L} - 2L_{\rm INT}$, where $X_{\rm L}$ is the channel length offset due to mask/etch effect, $L_{\rm INT}$ is the channel-length offset parameter. The characteristic length $L_{\rm t} = \sqrt{\frac{\epsilon_{\rm si}}{\epsilon_{\rm ox}}T_{\rm ox}X_{\rm dep}}$, where $\epsilon_{\rm si}$,$\epsilon_{\rm ox}$ are the dielectric constants of silicon and silicon-dioxide respectively, $T_{\rm ox}$ is the gate oxide thickness. The depletion width $X_{\rm dep} = \sqrt{\frac{2\epsilon_{\rm si}\phi}{qN_{\rm dep}}}$, where $\phi = 2\frac{kT}{q}\ln\left(\frac{N_{\rm dep}}{n_{\rm i}}\right)$, $N_{\rm dep}$ is the channel doping concentration at depletion edge for zero body bias, and $n_{\rm i}$ is the intrinsic carrier concentration in the channel region.

From Equations (1–3), the noise rejection curve can be predicted for any values of different parameters — gate length, L, threshold voltage, $V_{\rm T}$, gate size, W, and supply voltage $V_{\rm DD}$ by using the exponential capacitance charge/discharge equations, as done in [8]:

$$\Delta_{\rm c} = R_{\rm eq}C_{\rm eq}\ln\left[\frac{V_{\rm DD} - V_{\rm f}}{(1-\eta)V_{\rm DD} - V_{\rm f}}\right]. \quad (4)$$

IV. Results

We verify the accuracy of the developed model by comparing the results with SPICE simulation results. For the purpose of simulation, we used the predictive technology models for the 65nm node [11]. The value of η, as described in Section II, is 25% for the experiments described in this section. Figure 2 shows the comparison for variation in $L_{\rm eff}$ by 20%. The drawn lengths are indicated in the figure and the lengths of the PMOS and NMOS transistors have been assigned values at two opposite extremes. As mentioned in Section III, the existence of DIBL makes it more difficult to capture the impact of $L_{\rm eff}$ on the pull-up and pull-down resistances. The good agreement of the predicted and simulated results show that our model can capture DIBL effect due to $L_{\rm eff}$ variation.

The combined impact of $V_{\rm T}$ and $V_{\rm DD}$ variations is depicted in Figures 3 and 4 for two arbitrary values of $V_{\rm DD}$ for

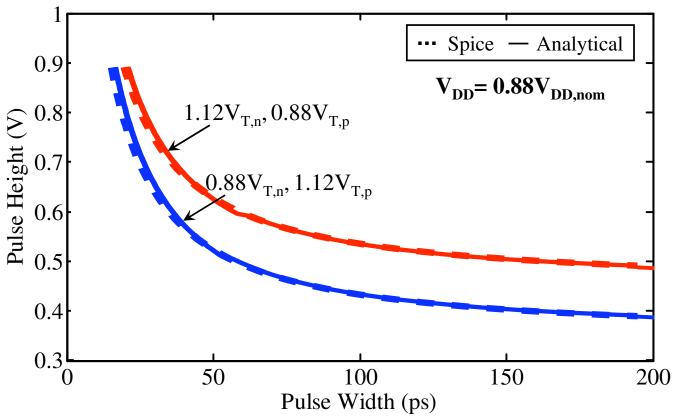

Figure 3. Comparison of the predicted and simulated NRCs for different combinations of $V_{\rm T}$ for $V_{\rm DD} = 0.88V_{DD,nom}$.

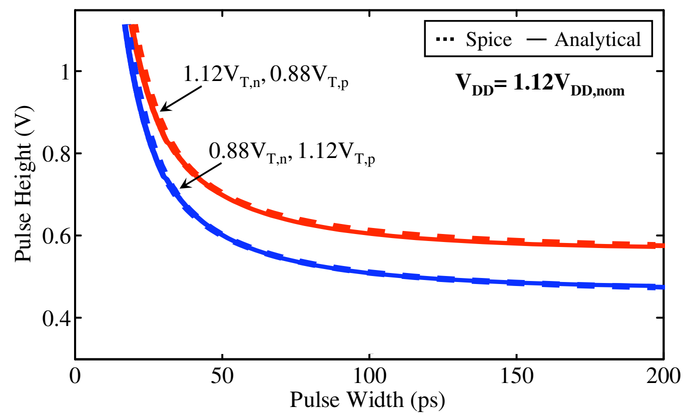

Figure 4. Comparison of the predicted and simulated NRCs for different combinations of $V_{\rm T}$ for $V_{\rm DD} = 1.12V_{DD,nom}$.

two values of $V_{\rm T}$. Good agreement between the predicted and simulated results can be seen here as well. Next we demonstrate that our model works as good for variations in multiple parameters, namely the $L_{\rm eff}$ and $V_{\rm T}$. We predict the two corner cases (the best and worst cases for rising input noise pulse) for 20% $L_{\rm eff}$ variation and 15% $V_{\rm T}$ variation by choosing appropriate values for the parameters. Figure 5 shows that the predicted corner NRCs match very well with the simulated NRCs.

We determine the noise susceptibility metric (ψ) by using trapezoidal integration of the points on the noise rejection curves. To quantify the error associated with the analytical predictions, we took four simulation points on each axis of a five-dimensional space: ($L_{\rm eff,n}$, $L_{\rm eff,p}$, $V_{\rm T,n}$, $V_{\rm T,p}$ and $V_{\rm DD}$) resulting into 1024 simulation points. The maximum variation in $L_{\rm eff}$ was 20%, whereas the maximum variations in $V_{\rm T}$ and $V_{\rm DD}$ were 15% each. The value of ψ was determined for each case from simulation as well as from the analytical NRCs. It was found that the average error was 1.26% with a maximum value of 5.04%, as shown in Figure 6, proving the accuracy of our proposed model. For these 1024 cases, SPICE simulations required 171 minutes, while our technique took only 40 milliseconds, thereby achieving a speedup of more than five orders of magnitude.

V. Conclusions

We presented an accurate method for analytically deriving noise rejection curves under parameter variations. The method involves modeling of the pull-up and pull-down resistances using approximated BSIM4 model-based device equations. Comparison of analytical results with circuit simulation results showed that the variations of $L_{\rm eff}$, $V_{\rm T}$, $V_{\rm DD}$ and W were accurately captured with an average error of 1.26% and a speedup of more than five orders of magnitude. Independent parameter variations in the pull-up and pull-down paths can be addressed by this model which provides an alternative to time consuming Monte Carlo simulations.

References

[1] C. Visweswariah, "Death, taxes and failing chips," in *Proc. Design Automation Conference*, 2003, pp. 343–347.

[2] C. Visweswariah *et al.*, "First-order incremental block-based statistical timing analysis," in *Proc. Design Automation Conference*, 2004, pp. 331–336.

[3] R. Rao *et al.*, "Parametric Yield Analysis and Constrained-Based Supply Voltage Optimization," in *Proc. Intl. Symposium on Quality Electronic Design*, 2005, pp. 284–290.

[4] K. L. Shepard, V. Narayanan, and R. Rose, "Harmony: Static noise analysis of deep submicron digital integrated circuits," *IEEE Trans. Computer-aided Design*, vol. 18, no. 8, pp. 1132–1150, Aug. 1999.

[5] D. Rabe and W. Nebel, "New Approach in Gate-Level Glitch Modelling," in *Proc. of the Conference on European Design Automation*, 1996, pp. 66–71.

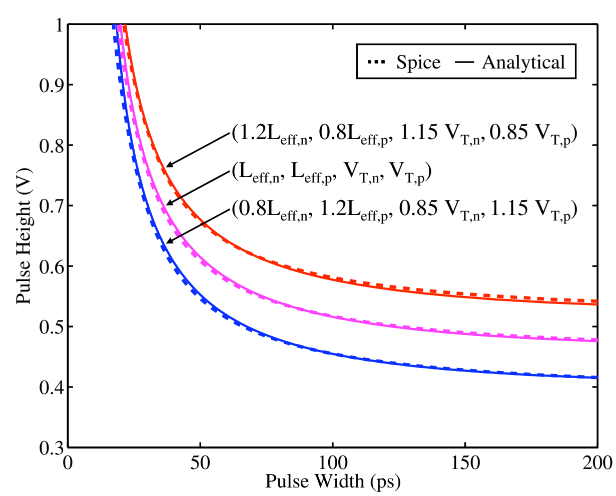

Figure 5. Noise rejection curves of an inverter for corner cases of $L_{\rm eff}$ and $V_{\rm T}$ variations. The parameters of the PMOS and NMOS transistors are varied separately.

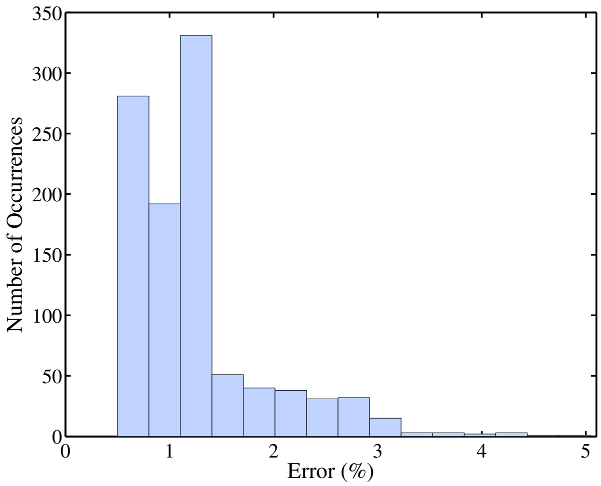

Figure 6. Error histogram for the presented analytical models.

[6] M. Saint-Laurent and M. Swaminathan, “Impact of Power-Supply Noise on Timing in High-Frequency Microprocessors,” *IEEE Trans. Advanced Packaging*, vol. 27, no. 1, pp. 135–144, 2004.

[7] M. Choudhury, Q. Zhou, and K. Mohanram, “Design Optimization for Single-Event Upset Robustness Using Simultaneous Dual-V_{DD} and Sizing Techniques,” in *Proc. Intl. Conference Computer-aided Design*, 2006.

[8] M. Mondal, K. Mohanram, and Y. Massoud, “Parameter-variation-aware analysis for noise robustness,” in *Proc. Intl. Symposium on Quality Electronic Design*, 2007. [Online]. Available: http://www.ece.rice.edu/∼kmram/publications/isqed07.pdf

[9] J. Rabaey, *Digital Integrated Circuits: a Design Perspective*. Prentice-Hall, Inc. Upper Saddle River, NJ, USA, 1996.

[10] M. V. Dunga, X. Xi, J. He, W. Liu, K. M. Cao, X. Jin, J. J. Ou, M. Chan, A. M. Niknejad, and C. Hu, *BSIM4.6.0 MOSFET Model*, Department of Electrical Engineering and Computer Sciences University of California, Berkeley, 2006. [Online]. Available: http://www-device.eecs.berkeley.edu/∼bsim3/BSIM4

[11] W. Zhao and Y. Cao, “New generation of predictive technology model for sub-45nm design exploration,” in *Proc. Intl. Symposium on Quality Electronic Design*, 2006, pp. 585–590. [Online]. Available: http://www.eas.asu.edu/∼ptm