Closed-form simulation and robustness models for SEU-tolerant design

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Abstract— **A closed-form model for simulation and analysis of voltage transients caused by single-event upsets (SEUs) in logic circuits is described. A linear RC model, derived using a SPICE-based calibration of logic gates for a range of values of fanout, charge, and scale factor is presented. A full set of experimental results demonstrate that on average, the model is accurate to within 5% of the results obtained using SPICE with over 100X improvement in computational speed. Besides simulation and analysis of SEU-induced transients, the proposed model can be used to perform reliability-aware logic synthesis through the incorporation of robustness metrics to tune cell libraries.**

I. Introduction

Technology trends, including smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth are projected to cause an increase in the soft error failure rate in nanoscale integrated circuits [2], [14], [15], [30]. Soft errors occur as a result of single-event upsets (SEUs) caused by high-energy neutron or alpha particle strikes in integrated circuits. Although soft errors cause no permanent damage, they can severely limit the reliability of electronic systems.

As design complexity increases, there is significant interest in the development of (i) simulation and analysis techniques for SEU-induced transients and (ii) SEU-robustness metrics for incorporation into the design flow at higher levels of design abstraction. In addition to the capability to simulate a range of SEU particle energies (charges), logic synthesis and design-for-reliability techniques require the capability to evaluate and optimize logic gates over a range of load and scale factors to meet design constraints. Such SEU-robustness metrics would facilitate convergence to inherently reliable solutions that meet area-delay-power objectives. This will not only lessen the investment in SEU analysis and hardening strategies in the latter stages of the design process, but also decrease the number of iterations in the design cycle.

Research in this direction has been hampered by the absence of efficient and accurate models for SEU-induced transients, primarily because of the non-linear nature of the differential equations. Whereas several approximations have been proposed and are discussed in Sec. II, there is no comprehensive model with a closed-form solution that is immediately usable not only for simulation, but also across the broad range of transformations that constitute logic synthesis. Such a unified model would have several advantages as soft error related concerns emerge even in mainstream cost-sensitive electronics [2].

This paper is a first step towards the development of a unified, accurate, and efficient closed-form model for (i) simulation and analysis of SEU-induced transients and (ii) SEU-robustness driven design-for-reliability techniques. The proposed approach resembles logical effort [23], [25] which is widely used to estimate gate and path delays in integrated circuits. A linear RC model, derived using a SPICE-based calibration of logic gates for a range of values of fanout, charge, and scale factor is introduced in this paper. The model has a closed-form solution for the SEU-induced transient, and can be integrated into simulation tools for soft error failure rate analysis. A full set of experimental results demonstrate that the model is accurate to within 5% of the results obtained using SPICE on average, with over 100X improvement in computational speed. The model is also compatible with load and performance constraints, and can be easily integrated into several design automation tools. Cell library synthesis and characterization tools can use the model for designing SEU-tolerant versions of cells subject to area-delay-power constraints. The model can also be used for back-of-the-envelope evaluations of soft error robustness, and can be used with logic synthesis tools to identify and harden highly susceptible gates in a design [29].

The rest of this paper is organized as follows. In Sec. II, we provide an extensive background and motivate the problem addressed in this paper in greater detail. In Sec. III, we describe the proposed model and derive closed-form solutions for the waveform of the SEU-induced transients. In Sec. IV, we present an algorithm to calibrate gates for the proposed model. In Sec. V, we present and discuss simulation results. Section VI is a conclusion.

II. Background and motivation

Current techniques for SEU-induced transient analysis and simulation fall into device-, circuit-, and logic-level categories depending on the extent of accuracy desired and the computational complexity. Device-level approaches take into account interactions at the nuclear level, and yield accurate results at exorbitant computational cost. Whereas these can be used to guide post-layout soft error analysis techniques, they cannot guide synthesis tools in the early phases of design space exploration. Examples include the work of [21] that formed the basis for many modeling programs such as [13] and the soft error Monte Carlo modeling program (SEMM) [17].

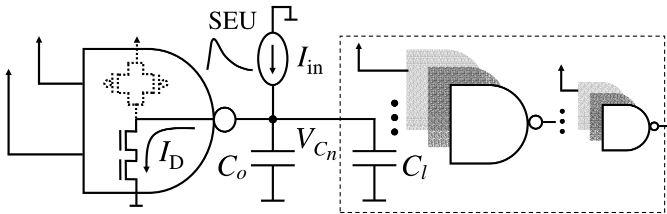

Fig. 1. Simulation setup for Fig. 2. A SEU modeled by a double exponential waveform I_{in} is injected at the output of a 2-input NAND gate, whose fault-free value is 1 (both inputs are high). Note that C_n equals $\xi(C_o + hC_l)$.

In contrast, circuit- and logic-level approaches use a double exponential model [6], [16], [24] for a SEU at a node (Eqn. 1, Sec. II-A). Logic-level approaches are abstraction-based, approximating SEU-induced transients by square pulses with equivalent magnitude-duration profiles. Such models are mainly used for fault injection and simulation, and compromise accuracy for speed of computation. Examples include linear regression modeling in the gate-level transient fault simulator described in [4] and square pulse modeling in [1].

Circuit-level approaches constitute the middle ground between device-level and logic-level simulation approaches. Empirically verified circuit-level models, such as [8], use scaling factors to extend the base model for a 600nm process technology to other feature sizes. SPICE-based circuit-level approaches, such as [27], depend on lookup table and databases for simulation. A second class of SPICE-based circuit-level approaches have focused on the solution to the transistor-level differential equation to obtain a closed-form solution for the SEU-induced transient at the output of a logic gate. This is a non-linear second-order Riccati differential equation. The absence of a particular solution for the initial conditions precludes the existence of a general closed-form solution. Numerical methods suggested in literature to solve this equation include the use of a computationally expensive infinite power series solution [22] and numerical analysis based on the fourth-order Runge-Kutta method [28]. In [6], the method from [22] was improved using piecewise quadratic functions to further improve the accuracy of simulation. In [5], a first-order RC model for pulse width computation, augmented by a set of rules for transient propagation was proposed in a switch-level simulator. In summary, previous research on circuit-level methods for SEU-induced transients are limited in their flexibility for the dual objectives of synthesis and simulation. The closed-form model proposed in this paper falls into the category of circuit-level techniques and overcomes these drawbacks. The model can be used to obtain both magnitude and duration of the transient waveform at a logic gate. In combination with transient fault propagation models such as [19], it can be used to accurately simulate SEUs in logic circuits. Further, the model integrates gate scale factor and load (through fanout) making it compatible with synthesis tools for SEU-robustness evaluation and design. The relative simplicity and high accuracy allow it to be used early in the design process to evaluate design alternatives.

A. Fanout, charge, scale factor, and process technology

Consider a 2-input NAND gate driving one or more identical 2-input NAND gates in its transitive fanout to two levels of logic that approximate loading conditions (described in Sec. IV). The charge deposition due to a particle strike at the output n of the NAND gate is modeled by a double exponential current pulse $I_{\text{in}}(t)$ at n [6], [16], [24]:

$$I_{\text{in}}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} \left(\mathrm{e}^{-t/\tau_\alpha} - \mathrm{e}^{-t/\tau_\beta} \right) \tag{1}$$

where Q is the charge (positive or negative) deposited as a result of the particle strike, τ_α is the collection time-constant of the junction, and τ_β is the ion-track establishment time-constant. τ_α and τ_β are constants that depend on several process-related factors. Note that $\lim_{t\to\infty} \int_0^t I_{\text{in}}(t)\mathrm{d}t$ equals Q for conservation of charge.

The output response of the NAND gate (determined using SPICE simulations) to a SEU that produces a $0 \to 1$ transient at the output—for combinations of values of fanout h, charge deposition Q, gate scale factor ξ, and process parameters τ_α and τ_β—is presented. Note that fanout is measured in terms of identical gates and the scale factor is uniformly applied to all transistors in the NAND gate and the fanout. A transient to logic 1 (logic 0) refers to the case when the steady-state logic value at n is logic 0 (logic 1) in the fault-free case and a SEU generates a positive (negative) transition to logic 1 (logic 0) at n. Both inputs of the NAND gate are set to logic 1, so that the voltage is 0 at n in the fault-free case. The worst-case transient occurs when the site for the particle strike is the gate output, since transients at internal nodes are reduced in severity before they propagate to the output of the gate.

In each sub-figure, it is clear that as the fanout h increases, the magnitude and duration of the SEU transient diminishes rapidly. For fixed h, ξ, τ_α, and τ_β, larger charges increase transient severity. Larger ξ (gate sizes) increase SEU-immunity and diminish SEU effects. Finally, the process parameter τ_α and τ_β also determine the magnitude and duration of the transients. Parameters h and ξ are central to post-mapping transformations such as gate resizing, fanout optimization, resynthesis and remapping, etc. [9] and hence are integral to the development of the unified model for simulation, analysis, and synthesis described in the next section.

III. Proposed three-parameter model $\tau_n(h, Q, \xi)$

The differential equation for the SEU-induced transient at the output of the NAND gate in Fig. 1 is given by:

$$C_n \frac{\mathrm{d}V_{C_n}}{\mathrm{d}t} = I_{\text{in}}(t) - I_{\text{D}}(t) \tag{2}$$

where C_n is the total load capacitance (load and parasitic) at n, $I_{\text{in}}(t)$ is the double exponential current pulse modeling the SEU, and $I_{\text{D}}(t)$ is the current through the nMOS transistor network restoring the output to its fault-free value. Note that C_n equals $\xi(C_o + hC_l)$, since ξ scales both the gate and its fanout. Since $I_{\text{D}}(t)$ is non-linear in V_{C_n}, the differential equation is equivalent to a non-linear second-order Riccati

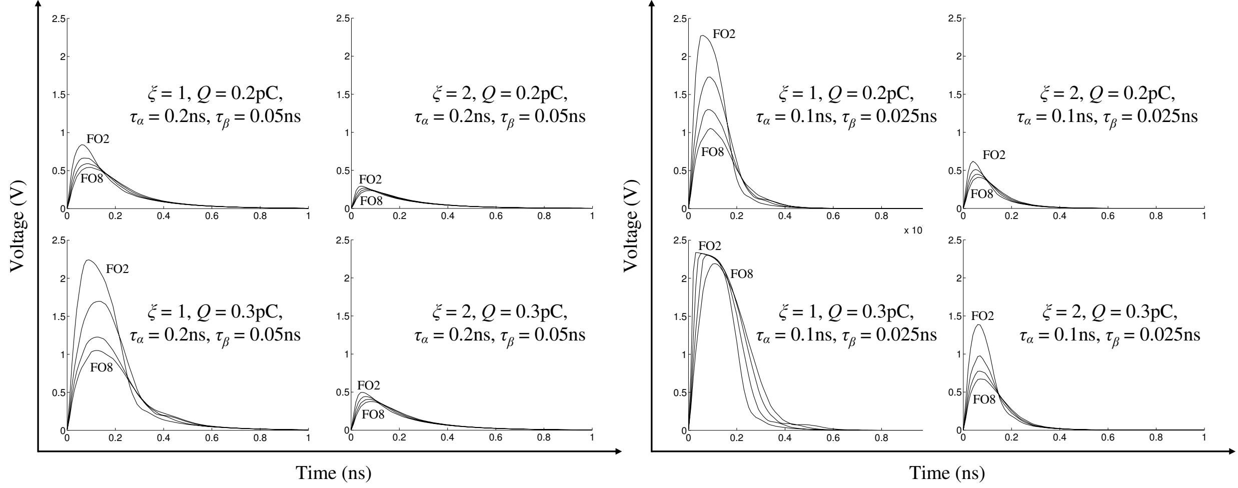

Fig. 2. Output transient as a function of fanout h, charge Q, scale factor ξ, and collection time-constant τ_α for a 2-input NAND gate in 130nm technology

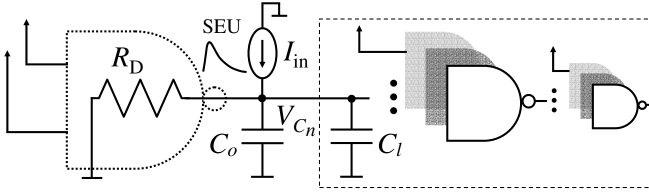

Fig. 3. Linear RC model for NAND gate when a particle strike occurs at its primary output. The nMOS transistor network is replaced by the equivalent resistance R_D.

differential equation with no closed-form solutions. Instead, we turn to the method of logical effort [23], [25], which has been widely used in a variety of application domains as well as in industry standard tools for electronic design automation. Logical effort is based on a reformulation of the conventional RC model of CMOS gate delay which separates the effects of gate size, topology, parasitics, and load. Using logical effort, the delay τ of a gate with input capacitance C_i is estimated by modeling it as a linear function of the load C_l being driven and is given by $gh+p$ where g is the logical effort, h equals C_l/C_i is the electrical effort (and hence fanout), and the parasitic delay p is the intrinsic delay of the gate.

Consider Fig. 3 that presents a similar linear RC model for the NAND gate from Fig. 1. R_D is the equivalent resistance that models the effects of the nMOS transistors that dissipate the charge and restore n to its original value. The product $R_\mathrm{D}C_n$ is denoted by τ_n, which can be thought of as a recovery time constant that reflects the ability of the transistors to dissipate the deposited charge to restore the node to its original logic value. Based on the discussions in Sec. II-A, the recovery time constant τ_n would be a function of the particle charge Q, the fanout h, and the gate scale factor ξ. A linear model for τ_n, along the lines for delay τ in logical effort, is given by:

$$\tau_n = a_0 + a_h h + a_Q Q + a_\xi \xi \qquad (3)$$

where a_0, a_h, a_Q, and a_ξ are constants determined using the calibration techniques described in Sec. IV.

With this model, the differential equation for the SEU-induced transient at the output of the NAND gate in Fig. 3 is given by:

$$C_n \frac{\mathrm{d}V_{C_n}}{\mathrm{d}t} = I_\mathrm{in}(t) - \frac{V_{C_n}}{R_\mathrm{D}} = I_\mathrm{in}(t) - \frac{C_n V_{C_n}}{\tau_n} \qquad (4)$$

We will return to the form $\tau_n = R_\mathrm{D}C_n$ in Sec. IV when we describe a methodology to calibrate the proposed model to obtain τ_n. A rearranged version of differential equation 4, shown on the left, is equivalent to the first-order differential equation of the form shown on the right.

$$\frac{\mathrm{d}V_{C_n}}{\mathrm{d}t} + \frac{V_{C_n}}{\tau_n} = \frac{I_\mathrm{in}(t)}{C_n} \equiv \frac{\mathrm{d}y}{\mathrm{d}x} + p(x)y = q(x) \qquad (5)$$

The solution to this first-order differential equation can be obtained through the use of integrating factors. The final solution to the transient waveform $V_{C_n}(t)$ is given by

$$V_{C_n}(t) = \frac{Q}{C_n \tau_\alpha} \mathrm{e}^{-t/\tau_n} \left(\frac{\mathrm{e}^{t/\tau_n} \cdot \mathrm{e}^{-t/\tau_\alpha} \big|_0^t}{1/\tau_n - 1/\tau_\alpha} \right) \qquad (6)$$

Without loss of generality, the parameter τ_β that controls the rise time of $I_\mathrm{in}(t)$ is ignored for the rest of this discussion. Note that all the analysis is easily extended to double exponential models for the injected current with non-zero τ_β and is presented in Sec. III-C.

A. $V_{C_n}(t)$ and $V_{C_n}(t_\mathrm{max})$

Depending on the relative values of τ_α and τ_n, there are five primary intervals in $\tau_n \in [0, \infty)$ that need to be analyzed in order to obtain the solution for the transient waveform. Further, except the limiting cases when τ_n equals 0 or ∞, it can be easily shown that the voltage $V_{C_n}(t)$ at the affected node changes from its steady-state value and reaches a peak value, before finally returning to its steady-state value. The

peak value that the node attains is obtained by differentiating Eqn. 6 and solving for the time instant $t_{\max}$ as follows:

$$t_{\max} = \begin{cases} \left(\frac{\tau_n \tau_\alpha}{\tau_n - \tau_\alpha}\right) \ln\left(\frac{\tau_n}{\tau_\alpha}\right) & : \tau_n > \tau_\alpha \\ \tau_\alpha & : \tau_n = \tau_\alpha \\ \left(\frac{\tau_n \tau_\alpha}{\tau_\alpha - \tau_n}\right) \ln\left(\frac{\tau_\alpha}{\tau_n}\right) & : \tau_n < \tau_\alpha \end{cases} \tag{7}$$

(i) $\tau_n = \infty$: This is a limiting case for dynamic nodes, since R_{D} is ∞ and the node is not driven. In this cases, the transient voltage $V_{C_n}(t)$ is an exponential function given by

$$V_{C_n}(t) = \frac{Q}{C_n}\left(1 - \mathrm{e}^{-t/\tau_\alpha}\right)$$

The maximum value of the voltage disturbance is given by $V_{C_n}(t_{\max}) = Q/C_n$, i.e., when all the charge is transfered to the capacitor. This is the model that would be used for DRAM cells as well as dynamic logic nodes.

(ii) $\tau_n > \tau_\alpha$: $V_{C_n}(t)$ is given by

$$V_{C_n}(t) = \frac{Q}{C_n}\frac{\tau_n}{(\tau_n - \tau_\alpha)}\left(\mathrm{e}^{-t/\tau_n} - \mathrm{e}^{-t/\tau_\alpha}\right)$$

Re-substitution of this value for $t_{\max}$ in the above equation gives the following expression for the peak value of $V_{C_n}(t)$.

$$V_{C_n}(t_{\max}) = \frac{Q}{C_n}\left(\frac{\tau_\alpha}{\tau_n}\right)^{\frac{\tau_\alpha}{\tau_n - \tau_\alpha}}$$

For the special case when $\tau_n >> \tau_\alpha$, the terms simplify to

$$V_{C_n}(t) \approx \frac{Q}{C_n}\mathrm{e}^{-t/\tau_n}\left(1 - \mathrm{e}^{-t/\tau_\alpha}\right) \text{ and}$$

$$V_{C_n}(t_{\max}) \approx \frac{Q}{C_n}\left(\frac{\tau_\alpha}{\tau_n}\right)^{\frac{\tau_\alpha}{\tau_n}}$$

In the limiting case, the behavior for $\tau_n >> \tau_\alpha$ approaches that of soft nodes above. The case $\tau_n >> \tau_\alpha$ is relevant for dynamic logic gates with a weak keeper, when the logic value may be fully corrupted following a particle strike, but is eventually restored by the keeper.

(iii) $\tau_n = \tau_\alpha$: In this case, the solution in Eqn. 6 is misleading since it seems to suggest that the charge can be dissipated as fast as it is deposited and that $V_{C_n}(t)$ is always 0. Using l'Hôpital's rule, or by direct integration of Eqn. 6 with τ_n equal to τ_α, $V_{C_n}(t)$ is given by:

$$V_{C_n}(t) = \frac{Q}{C_n \tau_n} t\mathrm{e}^{-t/\tau_n}$$

Here, $t_{\max}$ equals τ_α and $V_{C_n}(t_{\max})$ is given by:

$$V_{C_n}(t_{\max}) = \frac{Q}{C_n \tau_n}\tau_n \mathrm{e}^{-\tau_n/\tau_n} = \frac{1}{\mathrm{e}}\left(\frac{Q}{C_n}\right)$$

(iv) $\tau_n < \tau_\alpha$: $V_{C_n}(t)$ is given by

$$V_{C_n}(t) = \frac{Q}{C_n}\frac{\tau_n}{(\tau_\alpha - \tau_n)}\left(\mathrm{e}^{-t/\tau_\alpha} - \mathrm{e}^{-t/\tau_n}\right)$$

Substituting $t_{\max}$ from Eqn. 7 in the above expression gives the following expression for the peak value of $V_{C_n}(t)$:

$$V_{C_n}(t_{\max}) = \frac{Q}{C_n}\left(\frac{\tau_n}{\tau_\alpha}\right)^{\frac{\tau_\alpha}{\tau_\alpha - \tau_n}} \tag{8}$$

This is the most commonly encountered case for logic gates for nominal values of τ_α and is further discussed in Sec. V-D. For the special case when $\tau_n << \tau_\alpha$, which would be true for a large buffer, the terms simplify to

$$V_{C_n}(t) \approx \frac{Q}{C_n}\frac{\tau_n}{\tau_\alpha}\mathrm{e}^{-t/\tau_\alpha}\left(1 - \mathrm{e}^{-t/\tau_n}\right) \text{ and}$$

$$V_{C_n}(t_{\max}) \approx \frac{Q}{C_n}\left(\frac{\tau_n}{\tau_\alpha}\right)$$

(v) $\tau_n = 0$: This is again a corner case when the charge is dissipated as quickly as it is deposited. $V_{C_n}(t)$ is always 0 in this case.

B. *SEU-induced* $1 \rightarrow 0$ *transients*

The general solution for the voltage $V_{C_n}(t)$ following a $1 \rightarrow 0$ transient, when the voltage at a node transitions from V_{DD} to lower values and back to V_{DD} is given by:

$$V_{C_n}(t) = \begin{cases} V_{\mathrm{DD}}\left(1 - \frac{Q}{C_n}\left(1 - \mathrm{e}^{-t/\tau_\alpha}\right)\right) & : \tau_n = \infty \\ V_{\mathrm{DD}}\left(1 - \frac{Q}{C_n}\frac{\tau_n}{(\tau_n - \tau_\alpha)}\left(\mathrm{e}^{-t/\tau_n} - \mathrm{e}^{-t/\tau_\alpha}\right)\right) & : \tau_n > \tau_\alpha \\ V_{\mathrm{DD}}\left(1 - \frac{Q}{C_n \tau_n} t\left(\mathrm{e}^{-t/\tau_n}\right)\right) & : \tau_n = \tau_\alpha \\ V_{\mathrm{DD}}\left(1 - \frac{Q}{C_n}\frac{\tau_n}{(\tau_\alpha - \tau_n)}\left(\mathrm{e}^{-t/\tau_\alpha} - \mathrm{e}^{-t/\tau_n}\right)\right) & : \tau_n < \tau_\alpha \end{cases}$$

The expressions for $t_{\max}$ given in Eqn. 7 would still hold, though the time instant corresponds to a minimum $t_{\min}$ for the transients under consideration.

C. *Non-zero* τ_β

The parameter τ_β controls the rise time of the current pulse $I_{\mathrm{in}}(t)$ and is usually negligible in comparison to τ_α. Ignoring τ_β diminishes the severity of $I_{\mathrm{in}}(t)$ slightly and provides a conservative estimate for $V_{C_n}(t)$. Since the integrating factor used to solve Eqn. 5 is e^{t/t_n}, the general solution for $V_{C_n}(t)$ for non-zero τ_β is given by:

$$V_{C_n}(t) = \frac{Q}{C_n}\mathrm{e}^{-t/\tau_n}\left(\frac{\mathrm{e}^{t/\tau_n}\cdot\mathrm{e}^{-t/\tau_\alpha}\big|_0^t}{\tau_\alpha(1/\tau_n - 1/\tau_\alpha)} - \frac{\mathrm{e}^{t/\tau_n}\cdot\mathrm{e}^{-t/\tau_\beta}\big|_0^t}{\tau_\beta(1/\tau_n - 1/\tau_\beta)}\right)$$

There are several regions of interest, based on the relative values of τ_n, τ_α, and τ_β. For $\tau_\beta < \tau_n < \tau_\alpha$ (which is most relevant), $V_{C_n}(t)$ is given by:

$$V_{C_n}(t) = \frac{Q\tau_n}{C_n}\left(\frac{\mathrm{e}^{-t/\tau_\alpha} - \mathrm{e}^{-t/\tau_n}}{\tau_\alpha - \tau_n} - \frac{\mathrm{e}^{-t/\tau_n} - \mathrm{e}^{-t/\tau_\beta}}{\tau_n - \tau_\beta}\right)$$

It is important to note that there are no closed-form expression for the time instants $t_{\max}$ and $t_{\min}$ in this case, since $\mathrm{d}V_{C_n}/\mathrm{d}t = 0$ results in a transcendental equation in t.

IV. Calibrating the Model

The 3-stage calibration structure based on the 4-stage structure proposed in [25] for logical effort analysis is shown in Fig. 4. The two preliminary stages to shape the slope of the stimulus are replaced by a single first stage that contains the gate under calibration. A current source at the output (and not the input) of the gate under calibration serves as the stimulus. The second and third stages are there to serve as a load on

the first stage. Each stage contains a primary gate (a), a load gate (b), and a load on the load (c). Gate (c) is essential to model the gate-drain overlap capacitance and prevents the output of gate (b) from switching rapidly. Gate (a) in the first stage is the gate under calibration; its inputs have stabilized and its output is the site of a particle strike. All side inputs are set to non-controlling values to allow the propagation of the SEU-induced transient through the stages.

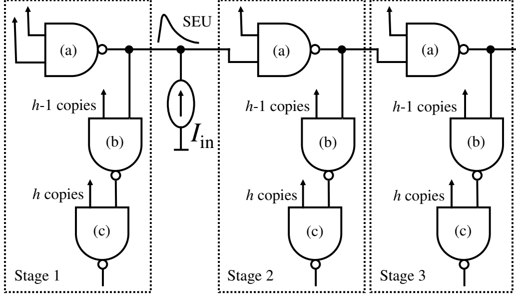

Fig. 4. Proposed test structure to calibrate the model.

For values of h, Q, and ξ, the calibration structure is simulated using SPICE over the interval $[0, \tau_\alpha]$. The value for τ_n is obtained from the simulation trace as follows. Consider the integral of both sides of Eqn. 4:

$$\int_0^{\tau_\alpha} C_n \frac{\mathrm{d}V_{C_n}}{\mathrm{d}t} \mathrm{d}t = \int_0^{\tau_\alpha} I_{\text{in}}(t)\mathrm{d}t - \frac{C_n}{\tau_n} \int_0^{\tau_\alpha} V_{C_n}(t)\mathrm{d}t \quad (9)$$

The term $C_n(\mathrm{d}V_{C_n}/\mathrm{d}t)$ corresponds to the current I_{C_n} through the capacitance C_n and its integral is given by the product of the measured average current through C_n and τ_α. Similarly, the average voltage across the capacitor V_{C_n} over the simulation interval is directly obtained from SPICE. The terms in Eqn. 9 can be rearranged to obtain τ_n:

$$\tau_n = \frac{C_n \int_0^{\tau_\alpha} V_{C_n}(t)\mathrm{d}t}{Q\left(1 - \mathrm{e}^{-t/\tau_\alpha}\right) - \int_0^{\tau_\alpha} I_{C_n}(t)\mathrm{d}t} \quad (10)$$

The pseudo-code for the procedure used to calibrate the gate in the test structure for a range of values on h, Q, and ξ is given in Fig. 5. Besides choosing a range of values for fanout h and scale factor ξ, the range of values for charge Q is determined by process-related factors as explained in Sec. IV-A. This produces a matrix of $\mathcal{M}$ of values obtained with a entry for τ_n corresponding to each combination of free variables (h, Q, ξ). Note that in Fig. 5, the dimensions of $\mathcal{M}$ are $(h_{\max}/2 \cdot 5 \cdot \xi_{\max})$ rows and 4 columns. Robust linear regression based on an iteratively re-weighted least squares algorithm (function `robustfit` in MATLAB) is then run on $\mathcal{M}$ to obtain the coefficients a_0, a_h, a_Q, and a_ξ. Further, in order to analyze the effects of process variations and to determine tolerance limits, τ_α can also be varied over a range of values and a separate calibration performed for each value in this range.

A. Choosing charge

Upper bounds on the charge used for calibration are determined as follows. The term linear energy transfer (LET) is

$h_{\max}$ – maximum allowed fanout for gate-under-calibration
$Q_{\max}$ – maximum calibration charge for process technology
$\xi_{\max}$ – maximum scale factor for gate-under-calibration
τ_α – junction collection time-constant for the process technology
$\mathcal{M}$ – $(h_{\max}/2 \cdot 5 \cdot \xi_{\max}) \times 4$ matrix with calibration entries

CALIBRATE-GATE($h_{\max}$, $Q_{\max}$, $\xi_{\max}$, τ_α);
for $h \leftarrow 2$ **to** $h_{\max}$ **by** 2
  for $Q \leftarrow Q_{\max}/5$ **to** $Q_{\max}$ **by** $Q_{\max}/5$
    for $\xi \leftarrow 1$ **to** $\xi_{\max}$
      do RUN-SPICE(h, Q, ξ, τ_α)
        $\tau_n \leftarrow$ COMPUTE-τ_n(h, Q, ξ, τ_α) ▷ Use Eqn. 9
        UPDATE($\mathcal{M}, \tau_n, h, Q, \xi$)
$(a_0, a_h, a_Q, a_\xi) \leftarrow$ RUN-LINEAR-REGRESSION($\mathcal{M}$)

Fig. 5. CALIBRATE-GATE($h_{\max}$, $Q_{\max}$, $\xi_{\max}$, τ_α)

used to describe the sensitivity of a process technology to SEUs. A particle with a LET of 1 MeV·cm^2/mg deposits approximately 10 fC/μm of electron-hole pairs along its track [7], [15]. The LET of very few ionizing particles in silicon is higher than 15 MeV·cm^2/mg [10], [26]. The LET of a particle is multiplied by the charge collection depth to obtain the total electron-hole pairs generated by a strike. For process technologies of 180nm and higher, the charge collection depth does not change significantly and is typically 2 microns in epitaxial (as well as bulk) substrates [11], [15]. This gives an upper bound of 0.3pC for 180nm process technologies. For smaller feature sizes, the charge collection efficiency decreases primarily due to higher channel doping density and a decrease in active layer thickness, which reduces depletion width and channel funneling [11], [12], [16]. In [8], an inverse linear relation between collected charge and doping density was determined empirically. For example, since uniform technology scaling [20] increases doping density by a factor of λ (equals $\sqrt{2}$) in successive process technologies, upper bounds of 0.21pC, 0.15pC, and 0.11pC can be derived for 130nm, 100nm, and 70nm process technologies. In Sec. V, we use the actual values of doping density to scale the base value of 0.30pC to obtain the calibration limit for smaller process technologies.

V. SIMULATION RESULTS

The SPICE libraries for four process technologies—180nm, 130nm, 100nm, and 70nm—were obtained from the Berkeley predictive technology model [3]. We used $\tau_\alpha = 0.2$ns and $\tau_\beta = 0$ in all our simulations. The maximum charges used for calibration of each process technology are presented in Table I. The charges were derived based on the discussion presented in Sec. IV-A. The doping densities for the n-channel were obtained from the SPICE files and used to scale the base charge of 0.30pC for a 180nm technology.[1] Note that these values are only a guideline to determine the maximum charge for a process technology.

[1]The doping density for the 130nm process technology does not follow the scaling trend. However, for consistency, we did not alter this and used 0.30pC as the worst-case charge for the 130nm process technology.

TABLE I

MAXIMUM CHARGE USED FOR CALIBRATION

Process technology (nm)	Doping density (cm^{-3})	Charge (pC)
180	$5.9 \cdot 10^{17}$	0.30
130	$5.6 \cdot 10^{17}$	0.30[1]
100	$9.7 \cdot 10^{17}$	0.18
70	$12.0 \cdot 10^{17}$	0.15

A. Accuracy of the proposed model

Fig. 6 presents a comparison of the waveforms for the SEU-induced transients for a 2-input NAND gate in 100nm and a 3-input nor gate in 130nm process technologies. In all the cases, the dotted curves were obtained from SPICE simulations. The solid curves were obtained when the calibration technique from Sec. IV was used to estimate τ_n and the closed-form double-exponential solution was used to plot the voltage waveform. (ξ, Q) were set to (1, 0.18pC) and (3, 0.30pC) respectively. It is clear that the transient waveform obtained using that proposed model is accurate to within 5%, both in magnitude and duration, of the transient waveform obtained using SPICE simulations for values of fanout from 2 to 8.

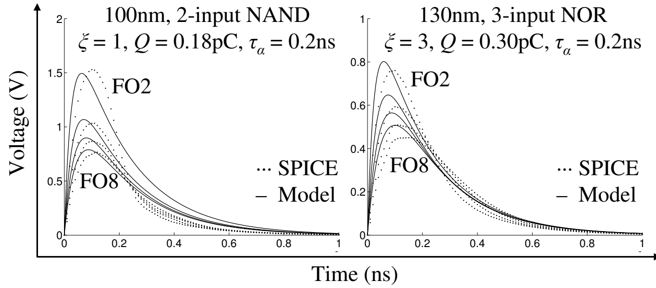

Fig. 6. Comparison of the simulation results for 100nm and 130nm technologies between the proposed model and SPICE

B. $\tau_n = a_0 + a_h h + a_Q Q$

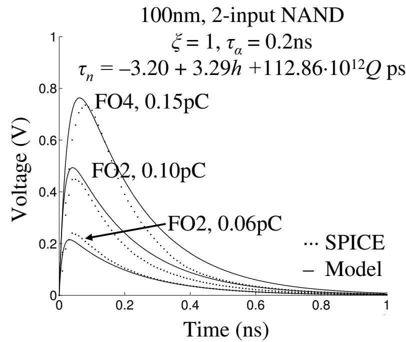

Fig. 7. Transient waveforms for 2-input NAND gate in 100nm technology. τ_n was calibrated as a function of fanout h and charge Q.

Fig. 7 presents the results for a 2-input NAND gate in 100nm technology when τ_n is modeled as a function of fanout h and charge Q. The calibration process explained in Sec. IV was performed using all possible pairs for $h = \{2, 4, 6\}$ and $Q = \{0.036, 0.072, 0.108, 0.144, 0.180\}$ pC. The solution for τ_n obtained following the calibration runs and linear regression is given in the figure. ξ was set to 1 for all the runs. The graphs shown in the curve are for three arbitrary pairs chosen in the the calibrated space, and it is clear that the transient waveform obtained using that proposed model (solid curves) is accurate to within 5%, both in magnitude and duration, of the transient waveform obtained using SPICE simulations (dotted curves) in all the cases.

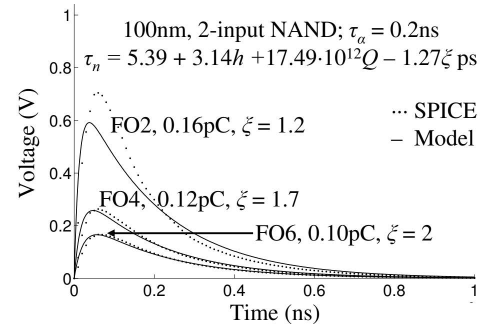

Fig. 8. Transient waveforms for 2-input NAND gate in 100nm technology. τ_n was calibrated as a function of fanout h, charge Q, and scale factor ξ.

C. $\tau_n = a_0 + a_h h + a_Q Q + a_\xi \xi$

Fig. 8 presents the results for the 2-input NAND gate in 100nm technology when τ_n is modeled as a function of fanout h, charge Q, and scale factor ξ. The calibration process from Sec. V-B was extended to include triples obtained using the values $\xi = \{1, 2, 3\}$. The solution for τ_n obtained following the calibration runs and linear regression is given in the figure. The graphs shown in the curve are for three arbitrary pairs chosen in the the calibrated space. For the $\{h = 2, Q = 0.16\text{pC}, \xi = 1.2\}$ triple, the results are off by approximately 15%. The main reason is that the triple is close to the boundary of the space that was calibrated. It is well known that such points are usually prone to larger errors in comparison to points chosen well within the space (as is the case with the other two curves). Hence, it is clear that the accuracy of the model can be improved by not only selecting more points within the calibration space, but also by extending the size of the calibration space to more than just the nominal points that occur in practice. Our experiments (that are not reported here) show that this significantly improves accuracy.

D. Design-for-SEU-robustness

With the proposed model, cell library synthesis and continuous, uniform gate sizing can be integrated to allow standard cell libraries to be automatically customized. For example, consider the 2-input NAND gate calibrated in Sec. V-C. Since V_{DD} is 1.2V for this process technology, SEU-induced transients can be prevented from propagating to fanout gates by limiting them to 0.6V at the site of the strike. A simple analytical procedure to determine the gate size ξ when the

NAND gate is robust enough to limit the peak of worst-case SEU-induced transients to 0.6V is as follows. For example, consider the case when the gate drives the equivalent of a fanout of 2. For worst-case charge 0.18pC, τ_n evaluates to 13.56ps for a unit-sized gate. C_n is 12.08fF in this case. Since $\tau_n > \tau_\alpha$, $V_{C_n}(t_{\max})$ is, from Eqn. 8, 0.83V. A similar calculation for ξ equals 2 shows that $V_{C_n}(t_{\max})$ is 0.38V. Thus, it is clear that a unit-sized gated is not robust to SEUs and that scaling it by a factor of 2 makes it robust. Using the bisection method [18] over the interval $\xi \in [1, 2]$, the exact size for the gate that limits the value of the SEU-induced transient to 0.6V (or any other voltage) can be determined. For this example, the optimum value for ξ is 1.35 to limit $V_{C_n}(t_{\max})$ to 0.6V. Note that scaling the gate reduces the equivalent fanout, and hence the load capacitance, since the sizes and topology of gates in the fanout remains unchanged. As a result, the value of 1.35 obtained above is a lower bound. If equivalent fanout is factored into the bisection-based search to further improve accuracy, the optimum value for ξ is 1.42 to limit $V_{C_n}(t_{\max})$ to 0.6V.

In this manner, the SEU-robustness metric can be incorporated during post-mapping transformations to render all (or a subset [29]) of the gates immune to worst-case SEUs. Note that gate sizing is conservative. This is because it attempts to limit transients locally and does not account for the attenuation that may occur along a propagation path. However, our experiments indicate that for the worst-case charges used for calibration, the SEU-induced transients are large enough that little or no attenuation occurs five levels of logic from the site of the strike on a sensitized path. Note also that since gate sizing for SEU-robustness impacts area, delay, and power, it can be used in combination with other gate sizing algorithms that target area-delay-power overhead objectives.

VI. CONCLUSION

In the future, as the soft error failure rate of logic circuits becomes unacceptably high even for mainstream applications, high-level SEU analysis and robustness techniques will play a critical role in accelerating convergence to SEU-tolerant designs. A closed-form, linear RC model that is accurate in comparison to SPICE at significantly less computational cost was presented in this paper. The model can also be used to continuously size gates to make them immune to worst-case SEUs for a process technology. An area for future research is to investigate how the proposed model can be integrated with other technology-dependent optimization algorithms with multiple objectives of area, delay, and power.

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