

Design optimization for robustness to single-event upsets

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Abstract: An optimization algorithm for the design of combinational circuits that are robust to single-event upsets (SEUs) is described. A simple, highly accurate model for the SEU robustness of a logic gate is developed. This model is integrated with area and performance constraints into an optimization framework based on geometric programming for design space exploration. Simulation results demonstrate the design tradeoffs that can be achieved with this approach.

1. Introduction

Technology trends, including smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth are projected to cause an increase in the soft error failure rate in sub-100 nm integrated circuits [1]–[5]. Soft errors occur as a result of single-event upsets (SEUs) caused by high-energy neutron or alpha particle strikes in integrated circuits. Although soft errors cause no permanent damage, they can severely limit the reliability of electronic systems.

Although cost-effective design as well as error detection and correction solutions for soft error robustness in memories, flip-flops, and latches have been proposed in literature [3], [6], [7], there are relatively few techniques that are cost-effective for use in multi-level logic circuits. Their applicability to combinational circuits is limited owing to (i) the irregular multi-level structure of combinational logic that leads to very high design overhead and (ii) the high cost of error detection, correction, and recovery required to support such techniques.

Recently, optimization based on transistor and gate sizing has been shown to be a promising solution for the design of logic circuits that are robust to SEUs [8]–[11]. Sizing for robustness to SEUs provides sufficient drive strength at the most vulnerable gates to dissipate the charge deposited due to a SEU locally. In this manner, the effect of the SEU is prevented from propagating along functionally sensitized paths to the primary outputs, flip-flops, or latches and resulting in soft errors. Sizing and other circuit-level techniques that increase robustness to SEUs are very attractive (i) since they do not incur any overhead for error detection, correction, and recovery and (ii) since they can be used to complement other fault avoidance and fault detection/tolerance techniques such as the use of silicon-on-insulator substrates, error detection and correction hardware, etc.

State-of-the-art sizing techniques for SEU robustness proposed in literature rely on rank-and-optimize heuristics to reduce the soft error failure rate. Rank-and-optimize heuristics

usually minimize a design constraint at the expense of other design constraints. For example, in [11], the rank-and-size heuristics based on uniform transistor and gate sizing always resulted in an increase in the delay and power of the hardened design. This may be unacceptable, especially for high performance designs where there is no room for compromise during optimization to achieve robustness to SEUs. This motivates research in global optimization approaches that allow simultaneous tradeoffs between traditional objectives of area-delay-power and SEU robustness. Such approaches allow finer control over design overhead and also have the potential to reduce runtime complexity.

In this paper, a simple, highly accurate, and comprehensive model for the single-event upset robustness of a logic gate is developed. The model integrates factors such as transistor size W , supply voltage V_{DD} , and threshold voltage V_T that are central to post-mapping transformations such as gate resizing, fanout optimization, resynthesis and remapping, etc. [12] ensuring compatibility with global optimization flows. This model is integrated with area and delay constraints into a global optimization framework based on geometric programming (GP) for design optimization for robustness to SEUs. GP-based optimization approaches have been used with great success on problems in transistor and gate sizing, multi- V_T , and multi- V_{DD} optimization in literature [13]. Such robustness driven design techniques will not only lessen the investment in SEU analysis and hardening strategies in the latter stages of the design process, but also decrease the number of iterations in the design cycle. They are advantageous over rank-and-optimize heuristics that, although effective, may not provide the best design alternatives to choose from. Simulation results for several logic circuits in the 100 nm process technology are presented to show that the proposed technique reduces the soft error failure rate significantly – as estimated through coverage to sensitized faults – with minimal impact to overhead.

The rest of this paper is organized as follows. In Sec. 2, we describe the proposed model and derive closed-form size-for-SEU-robustness expressions for use in design optimization. In Sec. 3, we present the proposed optimization algorithm to design logic circuits that are robust to SEUs. In Sec. 4, we present and discuss simulation results. Section 5 is a conclusion.

2. Closed-form circuit-level SEU model

In this section, we use linear gate models to derive closed form expressions for the waveform of the SEU-induced transient. We extend this model to derive closed form expressions for the minimum transistor and gate sizes required to limit the magnitude of the SEU-induced transient to less than a pre-specified value at the site of the strike.

Consider a gate driving one or more identical gates in its transitive fanout to two (or more) levels of logic that approximate loading conditions. A SEU-induced transient to logic 1 (logic 0) refers to the case when the steady-state logic value at the output of the gate is logic 0 (logic 1) in the fault-free case and a SEU generates a positive (negative) transition to logic 1 (logic 0). The worst-case transient occurs when the site for the particle strike is the gate output, since transients at internal nodes are reduced in severity before they propagate to the output of the gate. Without loss of generality, the rest of this paper discusses only $0 \rightarrow 1$ SEU-induced transients; $1 \rightarrow 0$ SEU-induced transients can be analyzed in a similar manner by symmetry.

The charge deposition due to a particle strike at the output of the gate is modeled by a parameterized, double-exponential current pulse $I_{in}(t)$ at the output [14], [15]:

$$I_{in}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta} \right) \quad (1)$$

where Q is the charge (positive or negative) deposited as a result of the particle strike, τ_α is the collection time-constant of the junction, and τ_β is the ion-track establishment time-constant. τ_α and τ_β are constants that depend on several process-related factors. Note that $\lim_{t \rightarrow \infty} \int_0^t I_{in}(x) dx$ equals Q for conservation of charge.

The differential equation of the SEU-induced transient at the output of the gate is then given by

$$C_{out} \frac{dV_{out}}{dt} = I_{in}(t) - I_D(t) \quad (2)$$

where C_{out} is the total load capacitance (load and parasitic) at the output node, $I_{in}(t)$ is the model for the SEU, and $I_D(t)$ is the current through the transistor network restoring the output to its fault-free value.

The differential equation belongs to the class of non-linear second-order Riccati differential equations, since $I_D(t)$ is a non-linear function of the output voltage V_{out} . The absence of a particular solution for the initial conditions precludes the existence of a general closed-form solution. Numerical methods suggested in literature to solve this equation include the use of a computationally expensive infinite power series solution and numerical analysis techniques [15], [16].

Instead, we follow an approach along the lines of the linear gate modeling techniques proposed in [17], [18] to derive closed-form expressions for the waveform and peak of the SEU-induced voltage transients. The main difference and advantage of the approach described in this paper over prior work is that whereas prior work focused on waveform approximation in both the linear and saturation regions, the

proposed model focuses only on the linear region of operation. This approach is very effective when the primary goal is to determine the minimum gate size that reduces the magnitude of the SEU-induced transient at the output of the gate to less than a pre-specified value ηV_{DD} . Note that the nMOS transistor network of the gate is in the linear region of operation as long as ηV_{DD} is less than $(V_{DD} - V_T)$, where V_{GS} is assumed to be V_{DD} . Hence the current $I_D(t)$ can be approximated by V_{out}/R_{SEU} , where R_{SEU} is the equivalent resistance of the nMOS transistor network in the linear region of operation. Based upon this, the solution to Eqn. (2) is given by

$$V_{out}(t) = \frac{QR_{SEU}}{\tau_\alpha - R_{SEU}C_{out}} \left(e^{-t/\tau_\alpha} - e^{-t/R_{SEU}C_{out}} \right). \quad (3)$$

Note that although τ_β is ignored from here on for simplicity, the reader can find a complete discussion of the differential equations including the τ_β parameter in [18]. The peak value of the SEU-induced voltage transient V_{max} is obtained by differentiating the above solution, solving for t_{max} , and by resubstitution in Eqn. (3). Let $\mu \equiv \tau_\alpha/R_{SEU}C_{out}$ for ease of notation. Then,

$$V_{max} = \frac{QR_{SEU}}{\tau_\alpha} \mu^{\frac{1}{1-\mu}}. \quad (4)$$

Parameterized model for V_{max} : Parameterization of this model is achieved based upon simplification of the $\mu^{\frac{1}{1-\mu}}$ term and an equivalent linear model for the resistance R_{SEU} of the nMOS network. The function $\mu^{\frac{1}{1-\mu}}$ is well approximated by $k_\mu \mu^\gamma$ with a goodness of fit value of 0.98 over the range $1 \leq \mu \leq 10$. This range of values for μ corresponds to a gate delay between 13.8 ps and 138 ps, which is valid for current process technologies. In the linear regime of operation, the resistance R_{SEU} of the nMOS network can be modeled as

$$R_{SEU} = \frac{k_{nMOS}}{(V_{DD} - V_T)W} \quad (5)$$

where W is the gate size, V_T is the threshold voltage, and k_{nMOS} is a constant. Resubstitution of these expressions for $\mu^{\frac{1}{1-\mu}}$ and R_{SEU} in the expression (4) for the peak value the SEU-induced voltage transient at the output gives

$$V_{max} = k_\mu Q \tau_\alpha^{\gamma-1} \left(\frac{k_{nMOS}}{(V_{DD} - V_T)W} \right)^{1-\gamma} C_{out}^{-\gamma}. \quad (6)$$

Size W_{robust} for robustness: Without loss of generality, let $V_{max} \leq \eta V_{DD}$ for the SEU-induced transient to be dissipated locally without sufficient magnitude and duration to propagate through the fanout gates. Let W_{robust} be the minimum gate size that is required to achieve this objective. Upon simplification of the expression (6) using this inequality, the minimum gate size W_{robust} for SEU robustness is given by

$$W_{robust} = k(V_{DD} - V_T)^{-1} \left(\frac{Q}{V_{DD}} \right)^{1+\beta} C_{out}^{-\beta} \quad (7)$$

where $\beta = \frac{\gamma}{1-\gamma}$, and $k = k_{nMOS} \tau_\alpha^{-1} (k_\mu/\eta)^{1+\beta}$. Based upon this, the constraints for SEU robustness during the

optimization procedure described in Sec. 3 will be given by $W \geq W_{\text{robust}}$ for all (or a subset) of the gates in the design. In order to make the expressions in Eqn. (7) accurate in comparison to SPICE simulations, a three-parameter model for W_{robust} given by

$$W_{\text{robust}} = k(V_{\text{DD}} - V_{\text{T}})^{-1} \left(\frac{Q}{V_{\text{DD}}} \right)^{1+\beta_0} C_{\text{out}}^{-\beta_1} \quad (8)$$

is derived using SPICE-based calibration runs. The parameters k , β_0 and β_1 are obtained for each type of gate (inverter, 2-input nand, etc.) by data fitting the simulation results obtained from SPICE. The parameters β_0 and β_1 were found to lie in the interval $\{0.15, 0.3\}$ in our simulations. The main difference between the expressions Eqn. (7) and Eqn. (8) is that the parameters in Eqn. (8) are further tuned by SPICE simulations to increase the accuracy (from a maximum error of 8% to 3%).

Compact robustness model: In order to determine the W_{robust} for SEU robustness, it is necessary to use an upper bound for charge deposition as a figure-of-merit during design analysis and optimization to increase SEU robustness. This is called the worst case charge $Q_{\text{w-c}}$ and is defined as the maximum charge deposited by a particle strike for which SEU robustness is sought for a design. For a given $Q_{\text{w-c}}$, the optimum W_{robust} can be determined during design-space exploration. Although supply voltage V_{DD} and threshold voltage V_{T} can be varied using multi- V_{DD} and multi- V_{T} optimization, this is out of the scope of this paper. Thus, for a given $Q_{\text{w-c}}$, and fixed V_{DD} and V_{T} , the compact model for minimum size for SEU robustness is given by the following expression:

$$W_{\text{robust}} = k(C_{\text{out}})^{-\beta} \quad (9)$$

This expression is used to derive robustness constraints for all (or a selection) of the gates in the design in the optimization algorithm described in the next section.

3. Circuit optimization

In this section, an iterative algorithm that integrates sizing for SEU robustness constraints into a global optimization algorithm based on geometric programming (GP) is described. The use of circuit optimization techniques based on GP and generalized GP (GGP) can be traced back to the TILOS paper on optimum sizing for delay [19]. Such approaches have since been used with great success on problems in transistor and gate sizing, multi- V_{T} , and multi- V_{DD} optimization in literature [13].

GP for minimum area: It is possible to formulate the problem of design optimization for minimum area using gate sizing – subject to performance constraints on delay T_{spec} at the primary outputs – as follows. We term this \mathcal{AD} , the area-delay

optimization problem.

$$\mathcal{AD} : \text{Minimize design area } \sum_{i=1}^n W_i$$

Subject to the following constraints

$$\begin{aligned} \delta_i + T_j &\leq T_i & j \in \text{fanin}(i) \text{ and } i = 1, 2, \dots, n \\ W_{\min,i} &\leq W_i \leq W_{\max} & i = 1, 2, \dots, n \\ T_i &\leq T_{\text{spec}} & i \in \text{primary outputs} \end{aligned} \quad (10)$$

where

- 1) W_i is the size of the i^{th} gate,
- 2) δ_i is the delay of the i^{th} gate given by the following expression
$$\delta_i = R_i C_{\text{int},i} + (R_i/W_i) \left(\sum_{j \in \text{fanout}(i)} C_{\text{in},j} W_j + C_L \right)$$
- 3) T_i is the arrival time at the output of the i^{th} gate,
- 4) T_{spec} is a specified circuit delay,
- 5) R_i is the resistance of the unit scaled gate,
- 6) $C_{\text{int},i}$ is the internal capacitance of the unit scaled gate,
- 7) $C_{\text{in},j}$ is the input capacitance of the unit scaled gate, and
- 8) C_L is the load capacitance if the i^{th} gate is a primary output, 0 otherwise.

Here, W_i and T_i are the variables of \mathcal{AD} . Since the objective as well as the delay constraints are posynomial functions of the variables, \mathcal{AD} is solved using GP-based approaches [13]. Note that although we refer to transistor sizes and use W_i in the formulation, we limit ourselves to symmetric gate sizing in this paper. Thus, scaling a single transistor through W_i is equivalent to scaling all transistors (nMOS and pMOS) in the gate by the same ratio. Note also that the minimum size constraint $W_{\min,i}$ on each gate can vary. This is of use from a sizing for SEU robustness perspective and is explained in greater detail in Sec. 3.1. W_{\max} remains fixed for all gates since this is a global constraint imposed by physical layout. Finally, both dynamic and static power can also be modeled as posynomials and introduced as additional constraints into this formulation as follows [13]:

$$\begin{aligned} P_{\text{dyn}} &= \sum_{i=1}^n \alpha_{\text{sw},i} \left(W_i C_{\text{int},i} + \sum_{j \in \text{fo}(i)} C_{\text{in},j} W_j + C_L \right) V_{\text{DD}}^2 \\ P_{\text{stat}} &= \sum_{i=1}^n W_i I_{\text{leak},i} V_{\text{DD}} \end{aligned}$$

where $\alpha_{\text{sw},i}$ is the switching activity at the i^{th} gate and $I_{\text{leak},i}$ is the leakage current of the unit scaled i^{th} gate. However, we focus on area-delay optimization for SEU robustness and neglect power constraints for the rest of this paper. In the next sub-section, an iterative procedure that integrates sizing for SEU robustness constraints into the \mathcal{AD} optimization problem is described.

3.1. Optimization for SEU robustness

The SEU robustness constraints for minimum gate size were derived in Sec. 2. These constraints can be incorporated into

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W – Vector of gate sizes
for each gate  $i$  set  $W_{\min,i} = 1$ ;
do
  W = Solve  $\mathcal{AD}$ 
  if  $W_i < k_i(C_{\text{out},i})^{-\beta}$ 
    set  $W_{\min,i} = (k_i(C_{\text{out},i})^{-\beta} + W_{\min,i})/2 + \epsilon$ 
  until all  $W_i \geq k_i(C_{\text{out},i})^{-\beta}$ 

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Fig. 1. Solving problem \mathcal{ADS}

the conventional \mathcal{AD} problem formulation by introducing an additional constraint at each gate of the form:

$$W_i \geq k_i(C_{\text{out},i})^{-\beta} \quad i = 1, 2, \dots, n \quad (11)$$

where k_i is a constant for each type of gate (inverter, 2-input nand, etc.) and $C_{\text{out},i}$ is the total load capacitance at the output of the i^{th} gate. $C_{\text{out},i}$ is given by

$$C_{\text{out},i} = \left(W_i C_{\text{int},i} + \sum_{j \in \text{fanout}(i)} C_{\text{in},j} W_j + C_L \right) \quad (12)$$

that is an affine function. Since $\beta > 0$, Eqn. (11) for SEU robustness *does not* have a posynomial form for direct integration into the GP optimization problem \mathcal{AD} .

The following observation can however be leveraged to develop an iterative approach to solve problem \mathcal{AD} together with SEU robustness constraints. We term the iterative approach \mathcal{ADS} for the area-delay-SEU optimization problem. For given values of transistor widths following a run of \mathcal{AD} , $C_{\text{out},i}$ can be computed for each of the gates in the design. Using this, new lower bounds on W_i can be computed for each gate as $W_{\min,i} = k_i(C_{\text{out},i})^{-\beta}$. These new values on $W_{\min,i}$ modify the constraints for the next run to solve the optimization problem \mathcal{AD} .

The pseudocode for the iterative approach is given in Fig. 1. The quantity ϵ refers to a small increment that aids in termination of the iteration-based optimization flow. In the first iteration, we solve problem \mathcal{AD} with all $W_{\min,i}$ set to 1 or an appropriate value determined by the library used for synthesis and the process technology. At the end of the first iteration, some gates do not satisfy the constraints on W_i for SEU robustness. On the next iteration, $W_{\min,i}$ is increased for all those gates that did not satisfy the SEU constraints. This is repeated until all the SEU vulnerability constraints are satisfied. Note that $W_{\min,i}$ for each gate is increased in every iteration. Hence, $W_{\min,i}$ approaches $k_i(C_{\text{out},i})^{-\beta}$ and ensures that the iterative approach to solve problem \mathcal{ADS} terminates after a finite number of iterations, either with a solution or by declaring infeasibility.

3.2. Example

In order to illustrate the proposed iterative algorithm, we consider the example of a chain of 10 inverters and solve the \mathcal{ADS} optimization problem. The basic \mathcal{AD} problem for the

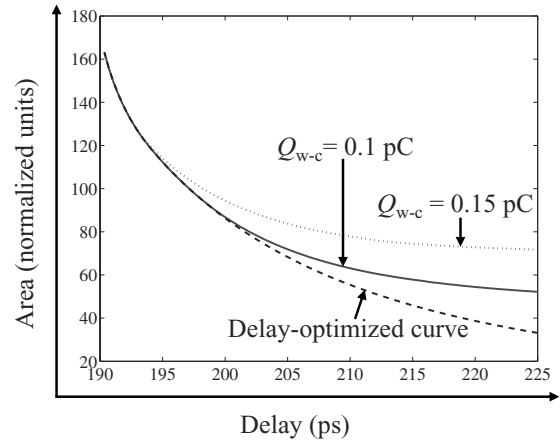


Fig. 2. This figure illustrates the area versus delay curves for a chain of 10 inverters in 100 nm technology. At large values of T_{spec} , the area of the design optimized for SEU robustness is greater than that of the delay-optimized circuit. Also, for the same T_{spec} , the overhead for a worst case charge Q_{w-c} of 0.1 pC is less than that for a Q_{w-c} of 0.15 pC. As T_{spec} decreases, the delay constraints dominate the SEU robustness constraints and the curves converge in both graphs.

chain of inverters is set up as follows:

$$\begin{aligned} & \text{Minimize design area } \sum_{i=1}^{10} W_i \\ \text{Subject to } & \begin{cases} \delta_0 \leq T_0 \\ \delta_i + T_{i-1} \leq T_i & i = 1, 2, \dots, 9 \\ W_{\min,i} \leq W_i \leq W_{\max} & i = 0, 1, \dots, 9 \\ T_9 \leq T_{\text{spec}} \end{cases} \quad (13) \end{aligned}$$

where δ_i equals $R_i C_{\text{int},i} + (R_i/W_i) C_{\text{in},(i+1)} W_{i+1}$. The SEU robustness constraints for the inverter chain are:

$$\begin{aligned} & W_i \geq k_i(C_{\text{out},i})^{-\beta} \quad i = 0, 1, \dots, 9 \\ \text{where } & \begin{cases} C_{\text{out},i} = C_{\text{int},i} W_i + C_{\text{in},(i+1)} W_{i+1} & i = 0, 1, \dots, 8 \\ C_{\text{out},9} = C_{\text{int},9} W_9 + C_L \end{cases} \end{aligned}$$

Fig. 2 illustrates the area versus delay curves for a chain of 10 inverters in 100 nm technology. The conventional area-delay curve is labeled the delay-optimized curve, The two other curves are obtained when the chain is optimized for SEU robustness with worst-case charges Q_{w-c} of 0.1 pC and 0.15 pC respectively. η is fixed at 0.5 in both cases.

At large values of T_{spec} , the inverters are near the minimum sized inverter and there is an overhead penalty to achieving SEU robustness. Note also that for the same T_{spec} , the overhead for a Q_{w-c} of 0.1 pC is less than the overhead for a Q_{w-c} of 0.15 pC. As T_{spec} is continuously reduced, all the inverters in the chain start increasing in size and one or more arrival time constraints in the optimization formulation begin to dominate the robustness constraints at one or more gates. Typically, since there is a gradual increase in inverter size from the primary inputs to the primary outputs, the delay constraints dominate the robustness constraints at the primary outputs and their immediate fanin. As T_{spec} decreases, the delay constraints dominate the SEU robustness constraints at all the gates in the chain and the robustness constraints are

trivially satisfied. At this point, the three curves converge as seen in the figure. Since the overhead for a Q_{w-c} of 0.15 pC is higher than the overhead for 0.1 pC, the curve for a Q_{w-c} of 0.1 pC merges with the base area-delay curve earlier.

4. Results

The geometric programming framework for circuit optimization was implemented using the optimization tool MOSEK [20]. The SPICE library for the 100 nm technology node was obtained from the Berkeley Predictive Technology Model [21]. The combinational benchmark circuits were chosen from the ISCAS85 and LGSynth91 suite [22]. We used $\tau_\alpha = 0.2\text{ns}$ [15] and a Q_{w-c} of 0.1 pC in all our simulations. We built a technology library that comprised inverters, and 2-input and 3-input nand and nor gates of different drive strengths for initial synthesis of the benchmarks. The optimization for SEU robustness was performed on these synthesized netlists. η was set to 0.5, so V_{\max} (V_{\min}) was $0.5V_{\text{DD}}$ for $0 \rightarrow 1$ ($1 \rightarrow 0$) SEU-induced transients.

Coverage: Sizing all the gates in a design is overkill for most applications, since the soft error failure rates of gates is asymmetric in its distribution [23]. In [11], we showed that a coverage metric given by

$$\text{Coverage (\%)} = 100 \left(\frac{\sum_{\text{(candidates } g_c)} P_s(g_c)}{\sum_{\text{(all gates } g)} P_s(g)} \right) \quad (14)$$

could be effectively used to select candidate gates g_c for SEU robustness constraints. Here, P_s is the probability of sensitization, i.e., the probability that there exists one (or more) functionally sensitized paths from the gate to the primary outputs, flip-flops, or latches. In other words, the coverage metric leverages the well known observation from testing theory that fault detectability can vary by orders of magnitude across a design. An efficient parallel pattern fault simulator was implemented to identify and rank the candidate gates g_c that contribute significantly to the soft error failure rate (as estimated through sensitization probability). When these candidate gates are sized to meet W_{robust} constraints, the percentage of propagated SEUs over all the cycles is reduced (in %) by an amount that equals coverage for the worst-case parameters.

Results: The results for design optimization of eight logic circuits from the ISCAS85 and LGSynth91 suite [22] is presented in Table 1. Under the first major heading, details about the circuits that were chosen: name, number of primary inputs, number of primary outputs, and number of gates are provided. Under the second major heading, the circuit function is reported. Note that we chose circuits that were purely logic or a mixture of logic and ALU for the experiments. Based on the above discussion, the results reported in this section targeted a coverage metric of 90% for SEU robustness.

Each of the next three major headings corresponds to the T_{spec} that was used for optimization. We chose the values for

T_{spec} such that the overhead for SEU robustness is reported for a highly optimized design in the third column. The T_{spec} values are then relaxed by 10% and 25% from this optimum and the overhead for SEU robustness is reported in the fourth and fifth columns respectively. In all three cases, the overhead for SEU robustness is reported w.r.t the total area of the design optimized using the conventional area-delay problem formulation (\mathcal{AD}) for that value of T_{spec} .

It is interesting to note that when the design is optimized for T_{spec} , a significant number of gates in the design have larger sizes in the base case. Hence, the overhead required to satisfy SEU robustness constraints is a smaller fraction of the area of the base \mathcal{AD} -optimized design. As we relax T_{spec} , there is a decrease in the average size of the gates required to meet delay constraints. In the term $k_i(C_{\text{out},i})^{-\beta}$ at a gate in the design, smaller gates on average imply that $(C_{\text{out},i})^{-\beta}$ is larger on average across the design. Hence, $W_{\text{robust},i}$ that is the minimum size of a gate to meet SEU robustness constraints increases. This in turn results in a larger value for W_i in the optimized design, and is observed in the larger overhead w.r.t the base case for slower designs (larger T_{spec}).

A second observation is that though there is an increase in percentage overhead of slower designs when they are made robust, the slower robust design has a total area that is less than that required for the fast robust design. For example, the robust versions of the largest design i10 require an area of 19008, 15855, and 15372 units to meet constraints of T_{spec} , $1.1 T_{\text{spec}}$, and $1.25 T_{\text{spec}}$ respectively. The reason for this observed behavior is that delay optimization targets gates along the critical path and sizes them in a manner such that robustness constraints are satisfied trivially at the gates. However, along non-critical paths, the area of gates remains relatively unaffected. The number of critical paths increases as T_{spec} decreases and a larger fraction of gates satisfy robustness constraints trivially. Thus the percentage overhead required for SEU robustness in high speed designs, i.e., low T_{spec} designs is lesser than the percentage overhead required for SEU robustness in slow designs, i.e., designs with high T_{spec} .

Finally, it is clear that the proposed algorithm provides the designer with several alternatives to choose from. A significant advantage is that optimization for SEU robustness can be combined with optimization for area-delay-power globally across the design, leading to optimal or near-optimal designs.

5. Conclusion

In the future, as the soft error failure rate of logic circuits becomes unacceptably high even for mainstream applications, optimizing designs for SEU robustness techniques will become critical. Since the proposed approach has significantly less overhead than approaches based on fault detection and tolerance, and since it also does not require any runtime support in hardware, it is an attractive option to reduce the soft error failure rate with minimal impact to performance.

Table 1
SEU robustness overhead for 90% coverage and 0.1 pC Q_{w-c}

Circuit (PIs, POs, Gates)	Function	T_{spec}		$1.1 T_{\text{spec}}$		$1.25 T_{\text{spec}}$	
		Base area	Robustness overhead (%)	Base area	Robustness overhead (%)	Base area	Robustness overhead (%)
b9 (41, 21, 107)	Logic	752	12.9	549	16.4	464	20.5
c880 (60, 26, 554)	ALU and control	3460	27.1	2470	32.4	2267	36.9
c499 (36, 7, 772)	Priority decoder	6132	23.7	3565	33.0	3137	39.8
c1355 (41, 32, 783)	Error correcting	4816	24.4	3413	32.2	3149	37.6
c1908 (33, 25, 906)	Error correcting	5171	26.8	3806	31.2	3627	33.1
c2670 (233, 140, 1012)	ALU and control	5384	19.4	4407	21.3	4124	23.5
c3540 (50, 22, 1498)	ALU and control	8485	30.5	6412	30.0	6056	32.5
i10 (257, 224, 3130)	Logic	15981	18.9	13098	21.0	12580	22.2
Average overhead (%)		—	23.0	—	27.2	—	30.8

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